TECHNICAL MANUAL

ORGANIZATIONAL MAINTENANCE MANUAL: AUTOMATIC DATA PROCESSOR EQUIPMENT MAINTENANCE GUIDED MISSILE AIR DEFENSE SYSTEM AN/TSQ - 73

This copy is a reprint which includes current pages from Changes 1 Through 12.

HEADQUARTERS, DEPARTMENT OF THE ARMY
31 OCTOBER 1978

Change

No. 12

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DEPARTMENT OF THE ARMY
Washing, D.C., *24 November 1995*

Organizational Maintenance Manual : Automatic Data Processor

Equipment Maintenance

GUIDED MISSILE AIR DEFENSE SYSTEM AN/TSQ-79

TM 9-1430-655-20-6, 31 October 1978, is changed as follows:

1. Remove old pages and insert new pages as indicated below. New or changed material is indicated by the applicable change number, i.e., Change 12, at the bottom of the page adjacent to the page number. Revised text will have a vertical bar in the margin next to the changed areas. Revised illustrations will have suffix change letter added to the identification number.

Remove Pages	Insert Pages
A/(B blank)	A/(B blank)
3-15 and 3-16	3-15 and 3-16
3-62.1 and 3-62.2	3-62.1 and 3-62.2
3-62.1/(3-64.2 blank)	3-64.1/(3-64.2 blank)
3-67 and 3-68	3-67 and 3-68
3-83 and 3-84	3-83 and 3-84
4-21/(4-22 blank)	4-21/(4-22 blank)
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2. File this change sheet in front of the publication for reference.

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01122

Distribution:

To be distributed in accordance with DA Form 12-32-E, Block 2346, requirement for TM 9-1430-655-20-6.

WARNING

DANGEROUS VOLTAGE

is used in the operation of this equipment

DEATH ON CONTACT

may result if personnel fail to observe safety precautions

Never work on electronic equipment unless there is another person nearby who is familiar with the operation and hazards of the equipment and who is competent in administering first aid. When the technician is aided by operators, he must warn them about dangerous areas.

Whenever possible, the power supply to the equipment must be shut off before beginning work on the equipment. Take particular care to ground every capacitor likely to hold a dangerous potential. When working inside the equipment, after the power has been turned off, always ground every part before touching it.

Be careful not to contact high-voltage connections when installing or operating this equipment.

Whenever the nature of the operation permits, keep one hand away from the equipment to reduce the hazard of current flowing through vital organs of the body.

WARNING

Do not be misled by the term "low voltage." Potentials as low as 50 volts may cause death under adverse conditions.

For Artificial Respiration, refer to FM 21-11.

EXTREMELY DANGEROUS POTENTIALS

greater than 500 volts exist in the following units:

Display console high voltage power supply

Display console CRT

WARNING

For emergencies requiring immediate shutdown of system power, press SYSTEM POWER OFF switch located on power cabinet power transfer unit. Observe that SYSTEM POWER ON indicator light goes off.

CAUTION

CMOS memories contain electrostatic sensitive devices requiring special handling to avoid electrostatic discharge damage. When removing and replacing memory cards, observe the following precautions:

a. Immediately prior to handling within the shelter, make physical contact with a grounded surface to discharge any possible buildup of static electricity.

b. Package the memory storage cards in electrostatic bags prior to removing from the shelter.

LIST OF EFFECTIVE PAGES

Insert latest change pages, dispose of superseded pages in accordance with applicable regulations.

NOTE: The portion of the text affected by the changes is indicated by a vertical line in the outer margins of the page.

Dates of issue for original and change pages are:

Original ..... 0 ..... 31 Oct 78
Change ..... 1 ..... 16 Mar 79
Change ..... 2 ..... 2 Sep 80
Change ..... 3 ..... 30 Sep 81
Change ..... 4 ..... 30 Nov 83
Change ..... 5 ..... 30 May 84
Change ..... 6 ..... 22 May 86
Change ..... 7 ..... 8 Oct 86
Change ..... 8 ..... 22 Jan 87
Change ..... 9 ..... 7 Aug 87
Change ..... 10 ..... 16 Mar 89
Change ..... 11 ..... 24 Jun 91
Change ..... 12 ..... 24 Nov 95

Page No.	*Change No.
a-b	6
A	12
B Blank	12
i	6
ii	8
iii	11
iv - v	6
vi Blank	6
1-1 - 1-2	11
1-2.1	6
1-2.2 Blank	6
1-3 - 1-6	6
2-1-2-4	6
2-5 - 2-16	0
2-17	2
2-18 - 2-21	0
2-22	11
2-23	6
2-24 Blank	6
2-25 - 2-26	6
2-27	0
2-28 Blank	0
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2-34	0
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2-36	0
2-37	6
2-38	2
2-39	6
2-40	1
2-41	0
2-42 - 2-45	8
2-46 Blank	8
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3-2-3-3	6
3-4	0
3-5	1
3-6	6
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3-12 Blank	6
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3-16	12
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3-26	9
3-27 - 3-30	0
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3-45	6
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3-86.9 3-86.10 Deleted	10
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4-12 4-13	6
4-14	9
4-15	6
4-16 Blank	6
4-17	6
4-18 Blank	6
4-19	2
4-20 Blank	2
4-21	12
4-22 Blank	12
A-1	12
A-2	12
A-3	12
A-4 Blank	12
Index 1 - Index 2	9
Index 3 - Index 7	11
Index 8 Blank	11

*Zero in this column indicates an original page.

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DEPARTMENT OF THE ARMY
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ORGANIZATIONAL MAINTENANCE MANUAL: AUTOMATIC DATA PROCESSOR EQUIPMENT MAINTENANCE

GUIDED MISSILE AIR DEFENSE SYSTEM AN/TSQ-73

TABLE OF CONTENTS

TABLE OF CONTENTS Continued

TABLE OF CONTENTS-Continued

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS Continued

LIST OF TABLES

CHAPTER 1

INTRODUCTION

Section I. GENERAL

1-1. Scope. This manual contains organizational maintenance information for the Guided Missile Air Defense System AN/TSQ-73 Automatic Data Processor (ADP) equipment (fig. 1-1). This manual is for use by personnel responsible for maintaining the ADP equipment. Chapter 1 provides physical and technical characteristics. Chapter 2 provides a theory of operation. Chapter 3 provides maintenance and fault isolation. Chapter 4 provides removal and replacement instructions.

1-2. Forms, Records, and Reports. Refer to DA PAM 738-750 for the use and completion of all forms required for operating and maintaining the equipment.

1-3. Destruction of Army Materiel to Prevent Enemy Use. If capture of this equipment appears imminent, or if the equipment must be abandoned, it should be destroyed to prevent enemy use. Destruction procedures should be carried out only on orders from the cognizant authority. Refer to TM 43-0002-21 for procedures required for destruction of the equipment and related system materiel. Recorded tape transport cartridges and classified manuals are priority items requiring destruction.

1-4. Reporting Equipment Publications Improvements. Reporting of errors and omissions and recommendations by the individual user for improving this publication is encouraged. Reports should be submitted on DA Form 2028. Recommended Changes to Publications, and forwarded to: Commander, U.S. Army Missile Command, ATTN: AMSMI-LC-ME-P, Redstone Arsenal, Alabama 35898-5238.

1-5. Reference. Refer to List of Applicable Publications TM 9-1425-655-L for a list of related publications and reference documents.

1-6. Abbreviations. Refer to appendix A for a lit of abbreviations used in this manual.

1-7. Official Nomenclature. AN/TSQ-73 system nomenclature associated with the equipment is listed in table 1-1. For further identification, cross-reference is provided for the common name used in this technical manual.

1-8. General. The ADP equipment for the AN/TSQ-73 system includes two Central Processing Units (CPUs), four 32K memory units, an Input/Output Unit (IOU), a buffer unit and 10 supporting power supplies. Part of the ADP equipment is the ADP status and control panel, which contains all of the indicators and controls required for operation of the ADP equipment. Peripheral devices used with the ADP equipment are the Keyboard Printer Unit (KPU), which provides manual access to the ADP during data processing, and the Magnetic Tape Units (MTUs), that function as bulk external memories and program input devices. These units combine to process radar and fire unit input data as required for the AN/TSQ73 system to perform its assigned mission of FU selection and weapon assignment.

Table 1-1. AN,TSQ.73 Official Nomenclature

Official nomenclature	Common name
Air Defense System, Guided Missile AN/TSQ-73	AN/TSQ-73 system (battalion configuration) AN/TSQ-73 system (brigade configuration)
Shelter. Electrical Equipment S-529/TSQ-73	System shelter (battalion configuration) System shelter (brigade configuration)
Console, Assault Fire Command, Guided Missile OJ-299/TSQ-73	Display console
Data Display Group OD-96/TSQ-73	Data Display Group (DDG)

Table 1-1. AN/TSQ-73 Official Nomenclature -Continued

Official nomenclature	Common name
Recorder-Reproducer, Guided Missile System, RD-449/TSQ-73	Magnetic Tape Unit (MTU)
Test Set, Electronic Circuit Plug-In Unit TS-3317/TSQ-73	Module Test Set (MTS)

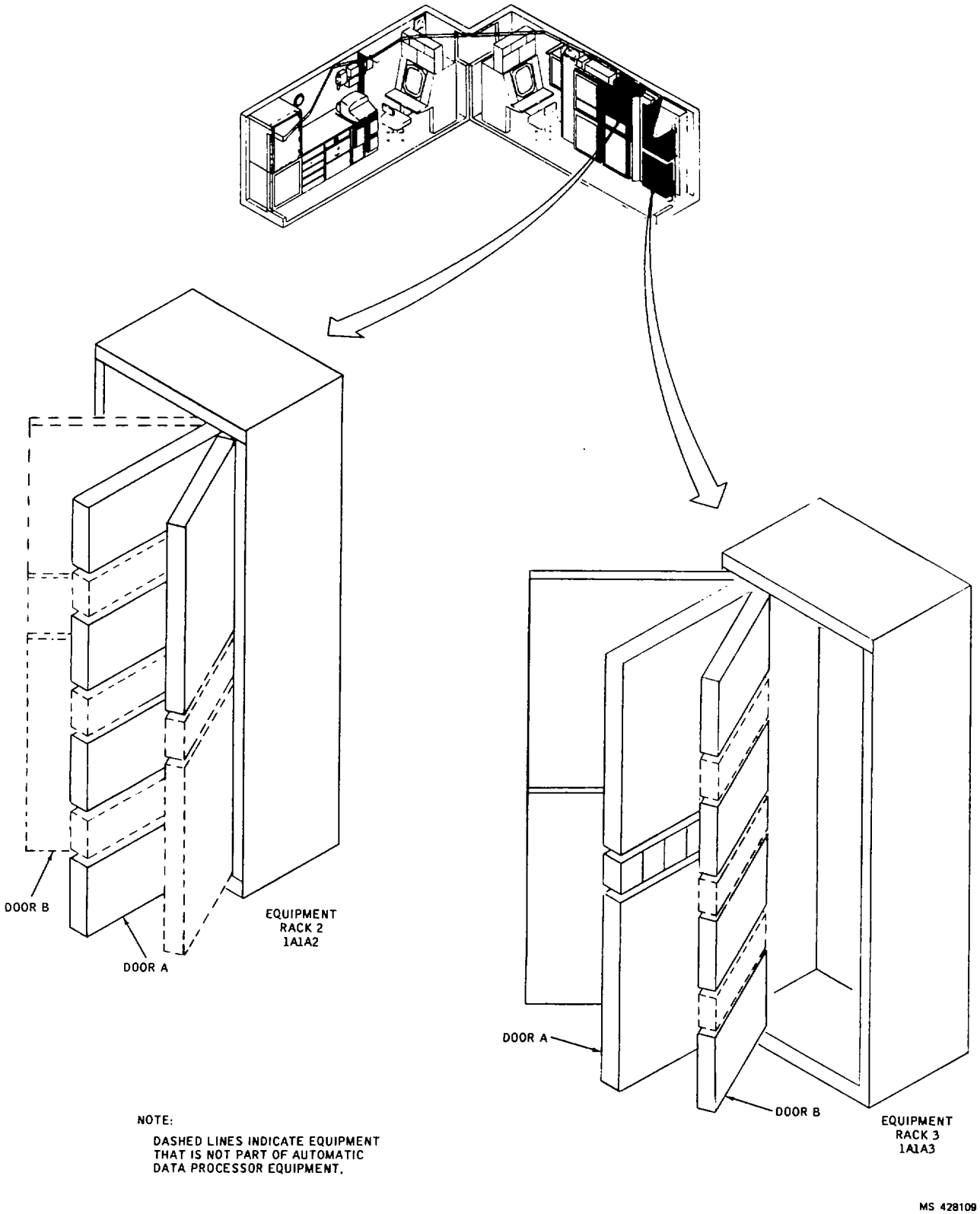

Figure 1-1. Automatic Data Processor Equipment

Section II. DESCRIPTION AND DATA

1-9. Physical Description. All of the ADP equipment is housed in equipment racks 1A1A2 and 1A1A3 (fig. 1-2). Each ADP unit is rack-mounted and connected to the system by cables which interconnect at the ADP interface panel. An ADP external interface panel is used for testing the ADP equipment.

a. *Central Processor Unit (CPU).* Each CPU contains two circuit card cages (bays) attached back-to-back. The bays are hinged at one edge for access to the wired backplanes. Electrical connections between the two card bays and other equipment are made through ribbon cables which plug into unused circuit card slots. Each bay has dc power applied through a separate cable connector from an associated dc/dc converter.

b. *32K Memory Unit (MU).* Each 32K MU has two circuit card cages with digital and analog cards. Electrical connections to other equipment are made through ribbon cables which plug into otherwise unused circuit card slots. Memory operating power is supplied by a dc power unit integral with each memory unit.

c. *Input/Output Unit (IOU).* The IOU has one circuit card cage. Access to the wired backplane is provided by a hinged panel. Signal connections to other equipment are made through ribbon cables which plug into unused circuit card slots. Dc power is applied through a separate cable connector from a dc/dc converter.

d. *Buffer Unit* The buffer unit contains the Display Output Unit (DOU) and has one circuit card cage. Access to the wired backplane is provided by a hinged panel. Signal connections to other equipment are made through ribbon cables which plug into unused circuit card slots. Dc power is applied through a separate cable connector from a dc/dc converter.

e. *DCIDC Converters*. Six dc/dc converters power the CPUs, IOU, and buffer unit. Each converter has one cable connector for dc input and one connector for dc outputs. Two fault indicators (one internal and one external) are provided on each converter.

f. *Deleted.*

g. *ADP Status and Control Panel* The ADP status and control panel houses the switches and indicators used to control the ADP equipment. Ribbon cables connect the panel to other ADP equipment.

1-10. Technical Description. The ADP equipment performs overall control and coordination functions for the AN/TSQ-73 system, and provides the necessary data processing for radar signals, simulation routines, the data communications terminal, and display data for the consoles, and also processes operator-initiated commands. The ADP equipment interfaces with the Radar Interface Equipment (RIE), display equipment, and data communications equipment, and provides these equipments with the necessary operating controls. Arithmetic, logic, and memory functions are performed during the data processing to interpret the various inputs for evaluation and action.

a. *Central Processor Units (CPUs).* Each CPU is a high-speed, general-purpose, microelectronic digital computer with approximately 100 defined instructions. An automatic diagnose instruction, initiated at power turn-on, provides Fault Isolation (FI) functions that complement the maintenance and diagnostic self-test software. The CPU uses high-speed TTL integrated circuits. The two CPUs form a dual-computer processing system that uses specially designed instructions for intercomputer communication. The CPUs are responsible for the arithmetic and control functions of the system. One of the two CPUs, which is designated as primary by the setting of an ADP status and control panel switch, processes the inputs and outputs. The other CPU is designated as secondary by the switch setting, and interfaces with the 32K memories only. If the designated primary CPU fails, the secondary CPU can be designated as primary with some loss of track processing. The data processing capacity of the ADP is reduced and longer processing times are required.

b. *32K Memory Units (MU).* Each of the four 32K MUs is a high-speed, high volume assembly that stores instructions and data words used by the ADP equipment. Each MU can store up to 32,768 words in complementary metal oxide semiconductor (CMOS) integrated circuit chips. The chips are replaceable and are set into removable circuit cards. Each memory has four independent controllers (ports) that connect to the two CPUs, the IOU, and the display output unit (DOU) of the buffer unit. Memory operation is in one of the four following modes: read, read/modify, write, and memory bank assignment/test.

c. *IOU*. The IOU regulates and controls the transfer of data between the primary CPU and the buffer unit. The IOU also performs the following operations not related to Input/Output (I/O) data transfer:

(1) Generates the time of day and times certain CPU functions using real-time clocks (RTC).
(2) Controls CPU and IOU power sequencing.
(3) Interfaces with ADP status and control panel.

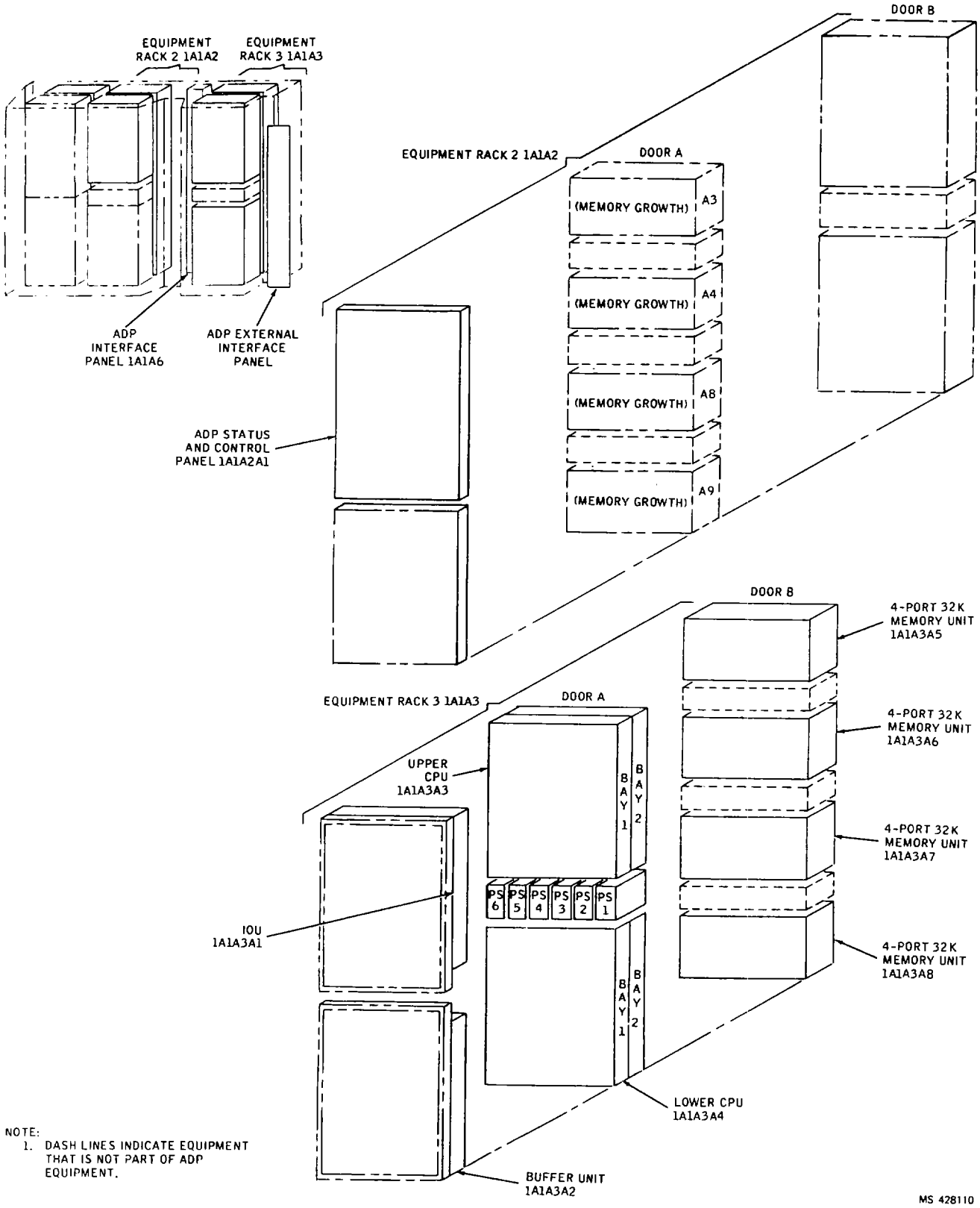

Figure 1-2. Automatic Data Processor Equipment Subassembly Location

d. *Buffer Unit.* The buffer unit regulates the transfer of data between the IOU and all peripheral devices, except the displays. Shelter-located peripherals (such as the Magnetic Tape Unit or the Keyboard Printer Unit) interface with one of two Input/Output Exchanges (IOXs). Each IOX interfaces with as many as eight peripherals. External communication peripherals (modulator-demodulator data links) interface with one of the five Input/Output Expanders (IOEs). Each IOE controls as many as four data links. The buffer unit contains a Display Output Unit (DOU). The DOU refreshes (updates) the shelter and remote displays. The displays receive refresh data directly from the 32K memory units through the DOU, allowing the CPU and IOU to devote all their functions to other peripheral devices.

e. *DC/DC Converters*. Each dc/dc converter transforms the shelter ± 135 vdc to the lower voltages required to power the ADP equipment logic circuits. A fault monitor circuit lights an indicator on the converter if an internal fault occurs. External voltage faults light a second indicator on the converter.

f. *Memory Power Supplies*. Each 32K MU is powered by an integral power supply that converts +135v to the lower voltages required by the memory unit logic circuits. A fault monitor circuit lights an indicator on the power supply if an internal fault occurs. The power supply generates the following voltages: +5v at 10A, -5v at 0.5A, and +12v at 0.75A. The power supply also generates an auxiliary +5v to power the POWER ON and POWER FAULT indicators on the control panel. If main power fails, 5-volt backup power is provided from the IBDL to ensure memory retention for 30 minutes.

g. *ADP Status and Control panel.* This panel contains all of the controls required to operate the ADP equipment, and also houses all of the ADP equipment indicators, except those on the dc/dc converters and memory power supplies. Three Light-Emitting Diode (LED) numerical displays are provided to aid in fault isolation.

h. *ADP Interface Panel.* The ADP interface panel is mounted on the shelter wall between equipment racks 1A1A2 and 1A1A3. The ADP interface panel provides connectors and wiring for connecting units of the ADP equipment and interfacing communications, display, and radar interface equipments.

i. *ADP External Interface Pane.* The ADP external interface panel contains provisions for connecting external computer test equipment to the ADP equipment for detailed test and troubleshooting procedures. The ADP external interface panel is located on the equipment rack installation between equipment rack 3 and the shelter door.

1-11. *Performance Characteristics*. Physical and technical characteristics of the ADP are listed in table1-2.

Table 1-2. Physical and Technical Characteristics

Item/function	Characteristics
Central Processor Unit:	
Instruction word length	32 bits
Data word length	1, 8, 16, 32, or 64 bits
Memory read/write cycle time	900 nsec
Memory features:	Access control and protection, and internal parity checking
Instructions:	100 basic instructions plus 50 extended mnemonic instructions
Addressing mode combinations:	9
Program levels:	64
Input/Output features:	Up to 126 I/O channels, each with program-initiated but independently operating data transfers of up to 32 bits in parallel I/O transfer rates of up to 400,000 32-bit words/sec on one channel or 180,000 32-bit words/sec when several channels are operating independently. A queue word for each program level provides stacking of interrupts

Table 1-2. Physical and Technical Characteristics --Continued

Item/function	Characteristics
Memory:	
Memory storage	Divided into banks. Each bank comprises 32,768 33-bit words (sixteen 2048 33-bit word pages)
Data word length	33 bits (32 data bits, one odd parity bit)
Access time	600 nsec
Read/write cycle time	900 nsec
Address word length	16 bits
Input/output priority	No. 1: IOU No. 2: CPU 1 No. 3: CPU 2 No. 4: DOU
Data storage type	Volatile (retained for 30 minutes with IBDL emergency power backup)
Special features	Internal self-test and fault isolation circuits
Buffer:	
Data word length	33 bits (32 data bits, one odd parity bit)
Input/output features	IOX and IOE data transmission rate up to 400,000 words/sec
DOU refresh rate	Displays refresh data at rate of 20 times/sec
DOU transmission rate	125,826 words/sec

CHAPTER 2

THEORY OF OPERATION

Section I. INTRODUCTION

2-1. Scope. This chapter provides a description of ADP Equipment functions. The ADP equipment includes two CPUs, four 32K memory units, an IOU, and a Display Output Unit (DOU). Peripheral devices used with the ADP equipment are the KPU, which provides manual access to the ADP during data processing, and two MTUs that function as bulk external memories and program input devices. These units combine to process the radar and fire unit input data as required for the AN/TSQ-73 system to perform its assigned mission of FU selection and weapon assignment. Figure 2-1 is a block diagram of the ADP subsystem.

2-2. ADP Functions. Major functions of the ADP are discussed in the following paragraphs.

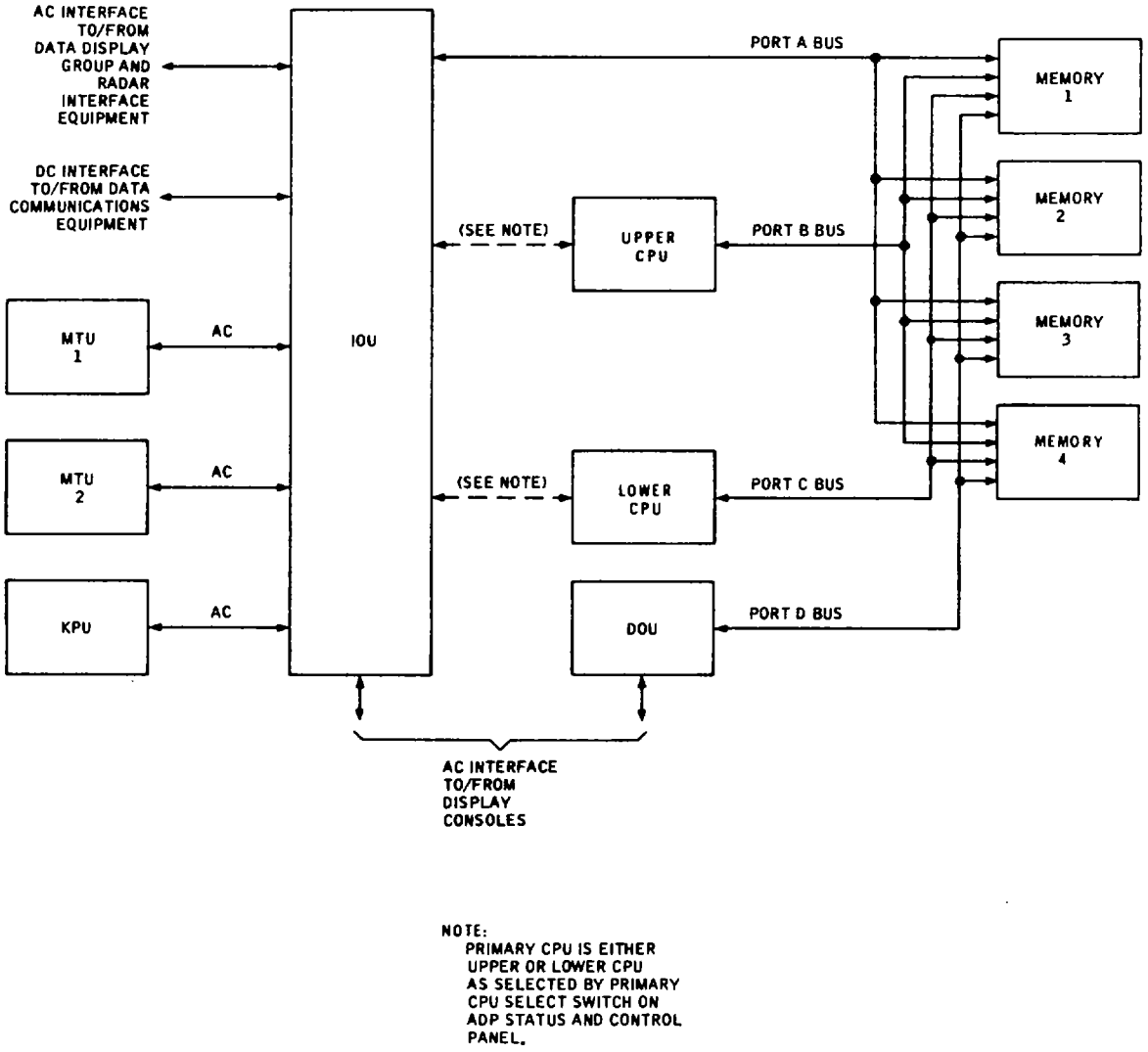

Figure 2-1. Automatic Data Processor Equipment Block Diagram

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Section II. PROCESSING FUNCTIONS

2-3. General. The processing function of the ADP equipment performs the logic, arithmetic, and memory operations that interpret inputs from the peripheral equipment, and controls the operation of those units. The processing function includes two CPUs and four 32K memory units (MU). One CPU is designated as primary by a front panel switch and processes the I/O function inputs and outputs. The other CPU is designated as secondary and interfaces only with the memories. If the designated primary CPU fails, the secondary CPU can be designated as primary. The data processing capacity of the ADP is reduced, however, and longer processing times are required. The four 32K MUs can be accessed by any of the units connected to the four ports on a time-shared basis. All data in a memory can be accessed from any port, permitting full memory access to all units.

2-4. Central Processor Unit (CPU) Basic Operation.

a. Operation During Program Execution. The following paragraphs provide descriptions of the basic operation of the CPU during program execution. Included in the CPU functions are instruction fetch, instruction interpretation, operand fetch, instruction execution, and terminate analysis.

(1) Instruction fetch. After a program has been loaded into memory and all initial conditions satisfied, the memory interface logic specifies the memory address of the first instruction programmed. The instruction word (32 bits) is read into the memory interface logic, and the command portion (bits 0 through 15) is transferred to the instruction controller logic. The second half of the word (bits 16 through 31), which is the operand address portion, is retained in the memory interface controller for future access.

(2) Instruction interpretation. The instruction controller logic interprets the command portion of the instruction word, and generates control signals that specify the operation, addressing mode, and process registers to be used. The operation control signals are used by the arithmetic logic to allow processing, and as sequence control for the rest of the CPU. The addressing mode signals are used by the memory interface logic if an operand must be obtained from memory and, if required, by the process register logic to select an index register. The process register select signal selects the accumulator in the process register logic which will be used during the operation.

(3) Operand fetch. The operand is the specific data addressed by the instruction word, and is generally accessed from the memory specified by the operand address stored in the memory interface logic and transferred to the arithmetic logic for implementation. If indexing is specified, the address mode signal from the instruction controller logic enables the readout of the designated index register from the process register logic. This readout is placed on the data bus and accepted by the memory interface logic to modify the existing operand address. The result, called the effective operand address, is used to obtain the operand. If indirect addressing modes are specified, the effective operand address is obtained through additional memory read cycles. The result then reads the operand from memory. If the literal addressing mode is specified, the operand address portion of the instruction word (stored in the memory interface logic) is read directly to the arithmetic logic as the operand. Where no operand is required, the stored operand address is used, if necessary, for additional control signals during instruction execution.

(4) Instruction execution. The instruction controller logic operation signal enables the process register selected by the process register select signal. The output of the process register is applied to the arithmetic logic where it is processed according to the operand. The resulting modified data is placed on the data bus for transfer to the memory or the active process register(s) for storage or use in following instructions. If the operation specified is a program level change, the data associated with the active program is stored in the memory and a transfer is made to the program level specified by the program level controller logic. The program level can also be changed when comparison of the active program with the next program gives the next program a higher priority. A priority compare signal is then generated, initiating the level change in the instruction controller logic. Once the instruction is complete, the control signals indicate a terminate condition.

(5) Terminate analysis. The terminate condition is a CPU state during which a decision is made concerning the next action to be performed. The selection is based on the following conditions, in decreasing priority:

(a) If a power-off condition exists, the power-off, level-change sequence is selected, regardless of other conditions.

(b) If an error condition exists (diagnose logic), the error exit level change is selected.

(c) If a trap condition exists, the next instruction is fetched from a specified process register. A trap condition exists when an arithmetic instruction is executed and the magnitude of the data numbers causes an overflow.

(d) If no level change is warranted, the next instruction of the active program is accessed (from memory through the instruction controller logic).

(e) If an interrupt has occurred (from input/ output (I/O) function, indicator line), a selection to determine the highest priority program level is initiated.

b. *Central Processor Unit (CPU) Logic Blocks Description* The following paragraphs contain general description of the logic blocks contained in the CPU (fig. 2-2).

(1) *Memory interface logic*. The memory interface logic controls the information flow between the CPU data bus and the 32K MUs. The functions of the memory interface logic include addressing the instruction word in memory and the data exchange to or from the addressed location. The memory interface logic also applies the command portion of the instruction word directly to the instruction controller logic and a control word, for comparison, to the diagnose logic.

(2) *Instruction controller logic*. The instruction controller logic is responsible for the orderly sequence of instruction execution. It interprets and retains the current instruction, determines the location of the next instruction, and retains indicator flags and error indicators for program use. The instruction controller logic also provides timing and control for instruction execution, controlling each step of the operation, and providing a comparison instruction to the diagnose logic for error checks.

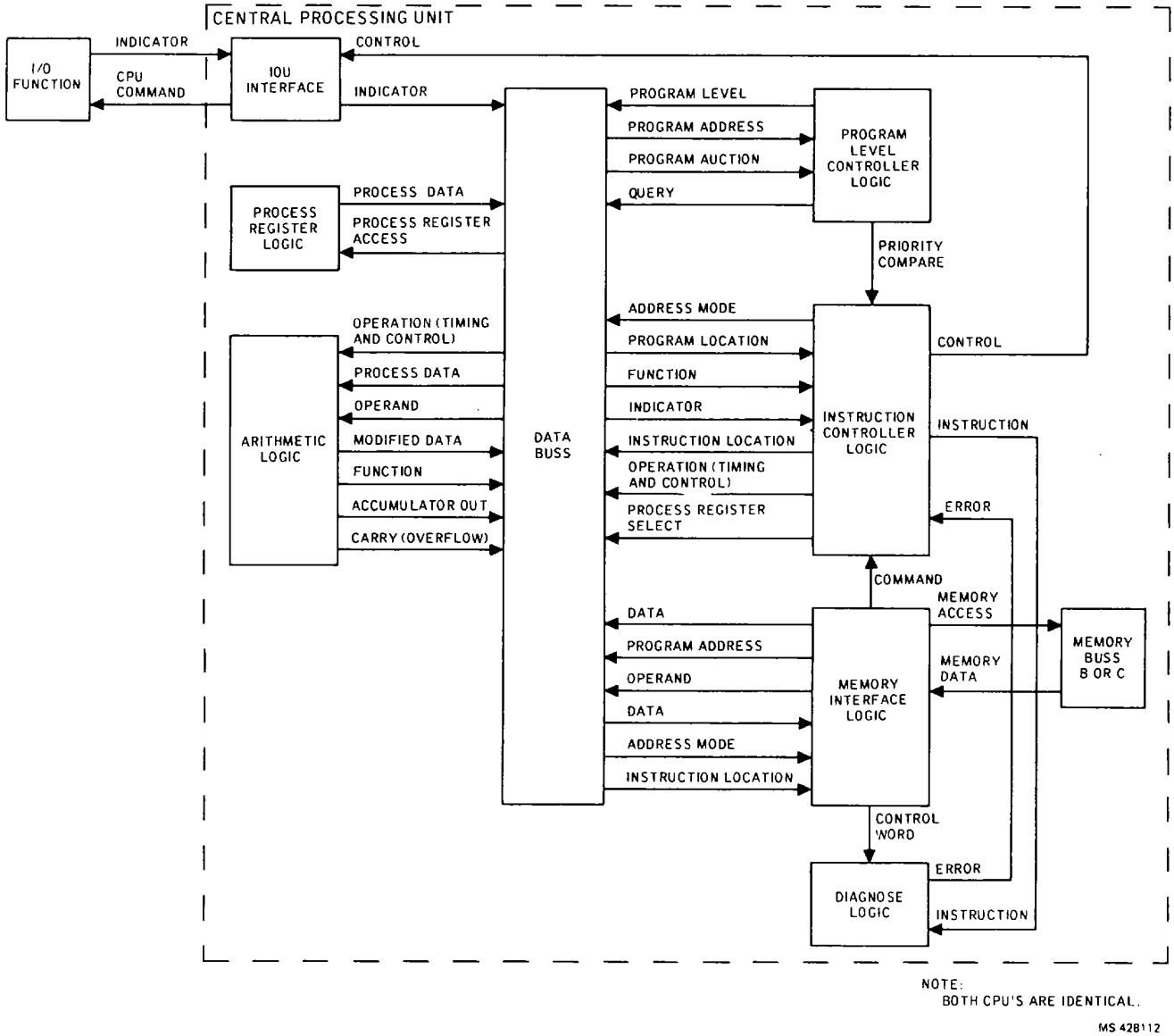


Figure 2-2. Central Processor Unit Block Diagram

(3) *Program level controller logic*. The program level controller logic supervises the sequencing and execution of all program level changes. It compares the priority of the active program level with the priority of the tentative program level and forwards that determination to the instruction controller logic. If a level change is indicated, the instruction controller logic initiates the change.

(4) *Diagnose logic* The diagnose logic performs the automatic fault detection and isolation function for the CPU. It performs a hardware test, forcing the CPU circuits to all ones or zeros and, if an error is detected, lights a corresponding front panel lamp and DIAGNOSE CODE readout corresponding to the maintenance and diagnostic (M&D) listings in the fault catalog.

(5) *Progress register logic* The process register logic consists of 16 registers on a semiconductor matrix The registers are used for temporary storage by the computer program as indicator and instruction location registers, accumulators, index registers, mask registers, and trap registers

(6) *Arithmetic log*. The arithmetic logic processes data from memory or active process registers as specified by the instruction controller logic operation signal. The arithmetic logic receives data from the data bus, performs algebraic, logical, or shift operations, and transmits the modified data over the data bus for storage either in the memory or the active process registers. If an overflow occurs in an arithmetic operation, the extra bits are read out to the data bus and stored in one of the process registers for action at a later time. The instruction controller is notified of the function taking place so that it can maintain control over the operations.

(7) *IOU* Interface The IOU interface facilitates communications between the CPU and I/O function, transferring the interrupt or acknowledge indicator signals to the CPU and the CPU command to the IOU.

2-5. Central Processor Unit (CPU) Detailed Description. A detailed description of the CPU is given in the following subparagraphs.

a *Functional Characteristic*. The CPU is functionally organized to provide the following;

(1) Processing of arithmetic, logical, data handling, and control instructions.

(2) Privileged instructions to permit control of memory protection, I/O operations, Real-Time Clock (RTC), and interrupts. Unauthorized use of a privileged instruction causes an interrupt.

(3) Semiprivileged instructions to permit control of program level communication. Unauthorized use of a semiprivileged instruction causes an interrupt.

(4) Arithmetic and logical operations on bits, bytes (8 bits), half words (16 bits), full words (32 bits); I/O operations on bytes and full words

(5) Priorities for up to 64 program levels and the capability to change from one level to another in response to an interrupt.

(6) A queue table that permits stacking of interrupts.

(7) Memory access protection so that memory cycles cannot be initiated unless appropriate access conditions are satisfied.

(8) Memory Bank Assignment (MBA) or test capability for two independent bank types.

(9) Addressing capability of 131,072 words of main memory.

(10) Parity generation and checking on memory data transfer.

(11) Program relocatability with efficient use of memory storage.

(12) Processing execution fault detection capability.

b. *Number Word Formats.* The CPU operates on half words, full words, and double words as shown in figure 2-3, A, B, and C, respectively. Numerical words have the following characteristics:

(1) Full words contain 32 bits, half words contain 16bits, and double words contain 64 bits.

(2) Numbers are processed as binary integers with negative numbers in two's complement form.

(3) Bit positions are assigned sequentially, left to right, with the Most Significant Bit (MSB) in the left-most position.

(4) The sign bit (S) is zero for positive numbers and one for negative numbers.

c. *Logical Word Formats*. The CPU can perform logical operations on data in the form of full words, half words, and 8 bit quantities (bytes). Figure 2-4, A and B, represent the logical word formats and figure 2-5, A and B, represent the byte positions in each half word.

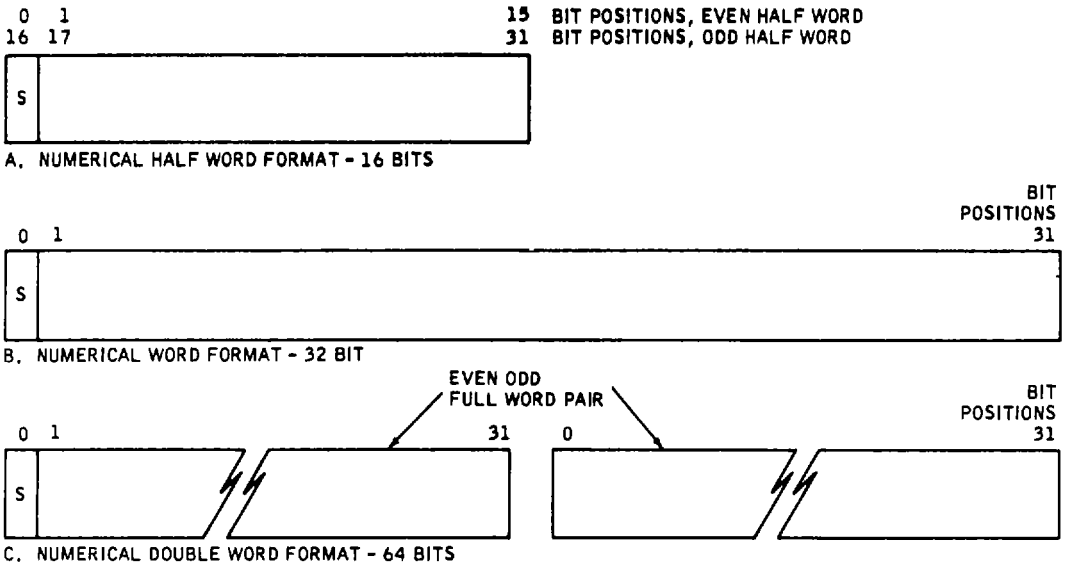


Figure 2-3. Numerical Word Format

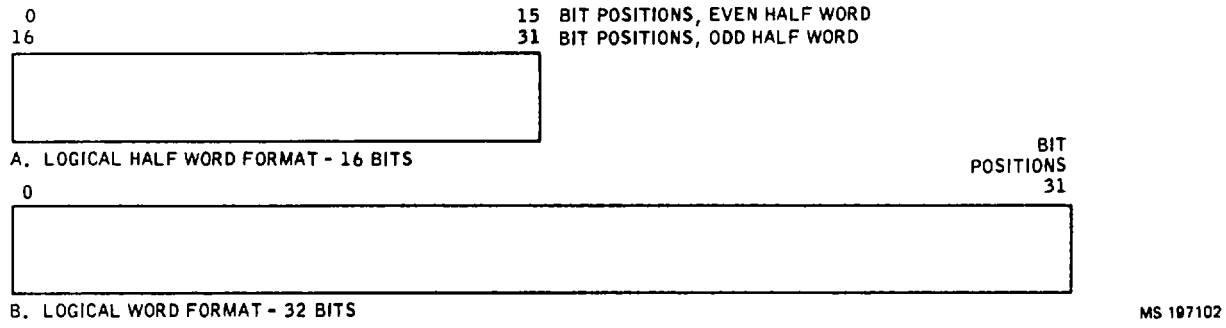


Figure 2-4. Logical Word Format

d. *Instruction Characteristics*. The instruction characteristics are as specified in the following subparagraphs:

(1) *Instruction Complement* One hundred instructions are provided, as listed in table 2-1.

(2) *Privileged Instructions*. Seven privileged instructions are provided and executed. When one of the instructions is used illegally, the instruction is not executed and an interrupt occurs.

(3) *Semiprivileged instructions*. Three semiprivileged instructions are provided and executed as specified in para 2-5. When one of the instructions is used illegally, the instruction is not executed and an interrupt occurs.

(4) *Trap instruction* When a nonimplemented code is encountered, the CPU traps by executing the instruction located in process register 178.

(5) *Instruction execution times.* The nominal execution times for the instruction set listed in table 2-1 applies for the direct addressing mode when no conflict exists for use of a memory bank due to an I/O data transfer.

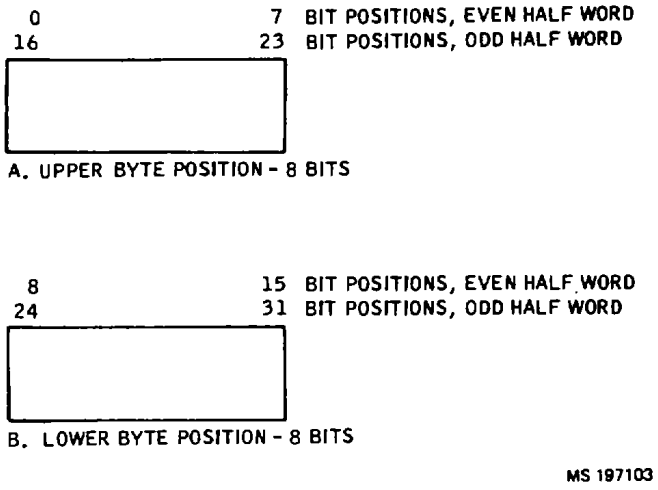


Figure 2-5. Byte Positions in Each Half Word

(a) Instruction execution time is increased by not more than 0.7 microsecond when the instruction's operand or indirect address is obtained from the same memory bank containing the instruction; 0.6 microsecond when using the relative address mode and the indexed address modes; 2.2 microseconds when using the indirect address mode; or the time required to complete an I/O data transfer that requires use of the same memory bank as the instruction.

(b) Instruction execution times are decreased by at least 0.9 microsecond when using the literal addressing modes and operands that address process registers.

(6) instruction word format The CPU uses a 32-bit instruction word with the format shown in figure 26. Normal use and definition of each instruction word held is as follows:

(a) Operand size (E), bit position 0. This 1-bit field generally specifies a 16-bit half-word operation or a 32-bit word operation (E=0 is a word operation, E=1 is a half-word operation).

(b) Operation (F), bit positions 1 through 6. This 6-bit field specifies the basic operation to be performed by the instruction.

(c) Addressing mode (M), bit positions 7 and 8. This 2. bit field provides four basic addressing modes which are expanded to the nine modes as specified in para 2-5d(7), according to the S-field values literal, direct, relative or indirect.

(d) Accumulator (H), bit positions 9 through 12. This 4-bit field selects one of 16 process registers to be used as an accumulator.

(e) Inder (S), bit positions 13 through 15. This 3-bit field selects one of seven process registers to be used for operand address indexing. The process registers are also addressable as accumulators with the H-field. S = 0 defines the non-indexed addressing modes.

(f) Operand address (CA), bit positions 16 through 31. The CA field is a 16-bit field that is either an operand in the literal address modes as specified herein, a special address as specified in (g) below, or a memory address, in which case it is divided into three subfields (D, A, and W).

(g) Special addresses For final operand or transfer addresses in the range of 000000 to 000077_8, the operand is located in selected registers as indicated in table 2-2 and as specified in para 2-5g. Privilege status required to modify registers selected by the special addresses are indicated in table 2-2.

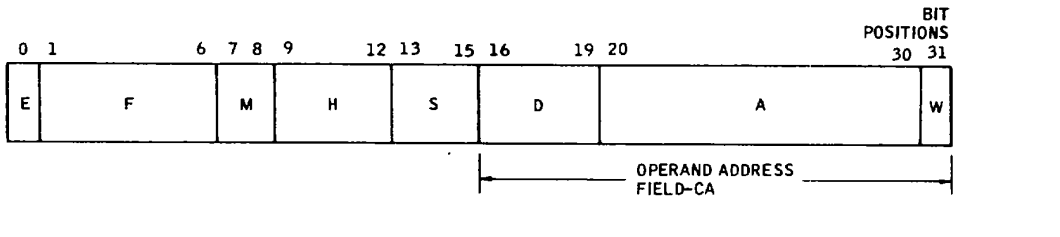


Figure 2-6. Instruction Word Format

Table 2-1. Instructions by Classes

Instruction					Nominal execution time* (microseconds)
Class	Subclass	Function code	Mnemonic	Name	
Arithmetic	Fixed-point Arithmetic	010	ADF	Add Full	4.8
		110	ADH	Add Half	4.8
		012	ALF	Add Logical Full	4.8
		112	ALH	Add Logical Half	4.8
		016	RAF	Replace Add Full	5.2
		116	RAH	Replace Add Half	5.2
		011	SBF	Subtract Full	4.8
		111	SBH	Subtract Half	4.8
		013	SLF	Subtract Logical Full	4.8
		113	SLH	Subtract Logical Half	4.8
		017	RSF	Replace Subtract Full	5.2
		117	RSH	Replace Subtract Half	5.2
		014	MPF	Multiply Full	16.4
		114	MPH	Multiply Half	16A
		015	DIF	Divide Full	18.1
		115	DIH	Divide Half	18.1
		033	RQF	Replace Square Root Full	16.6
	Compare	020	CMF	Compare Algebraic Full	4.7
		120	CMH	Compare Algebraic Half	4.7
		021	CLU	Compare Logical Upper Byte	4.8
		121	CLL	Compare Logical Lower Byte	4.8
		022	CLF	Compare Logical Full	4.8
		122	CLH	Compare Logical Half	4.8
		024	CSF	Compare Selective Full	5.6
		124	CSH	Compare Selective Half	5.6
		023	CGF	Compare Gated Full	5.4
		123	CGH	Compare Gated Half	5.4
		157	MTH	Modify and Test Half	4.8
Data Manipulation	Logic	025	IOF	Inclusive Or Full	4.7
		125	IOH	Inclusive Or Half	4.7
		035	RIF	Replace Inclusive Or Full	5.1
		135	RIH	Replace Inclusive Or Half	5.1
		026	EOF	Exclusive Or Full	4.7
		126	EOH	Exclusive Or Half	4.7
		036	REF	Replace Exclusive Or Full	5.1
		136	REH	Replace Exclusive Or Half	5.1
		027	ANF	Logical And Full	4.7
		127	ANH	Logical And Half	4.7
		037	RNF	Replace Logical And Full	5.1
		137	RNH	Replace Logical And Half	5.1
		057	SSF	Selective Substitute Full	5.7
	Format	030	FEF	Format Extract Full	5.3 + 0.12K**
		130	FEH	Format Extract Half	5.3 + 0.12K
		031	FIF	Format Insert Full	5.9 + 0.12K
		131	FIH	Format Insert Half	5.9 + 0.12K

*The direct addressing mode without indexing and the possibility of instruction-operand memory access overlap are assumed in the specification of the instruction execution times.
**K = bit positions shifted.

Table -2-1. Instructions by Classes – Continued

Instruction			Mnemonic	Name	Nominal execution time* (microseconds)
Class	Subclass	Function code			
Data Manipulation (continued)	Shift	032	SHF	Shift Full (and Double)	4.9 + 0.12K
		132	SHH	Shift Half	4.9 + 0.12K
	Set/Reset	034	SBT	Set Bit in Half Word	5.0
	Bit	134	RBT	Reset Bit in Half Word	5.0
Data Handling	Load	040	LDF	Load Full	4.5
	(Register)	140	LDH	Load Half	4.5
		044	LMH	Load Most Half	4.5
		041	LDU	Load from Upper Byte	4.5
		141	LDL	Load from Lower Byte	4.5
		042	LAF	Load Absolute Full	4.5
		142	LAH	Load Absolute Half	4.4
		043	LCF	Load 2's Complement Full	4.5
		143	LCH	Load 's Complement Half	4.5
	Store	046	SDF	Store Full	4.8
	(Register)	146	SDH	Store Half	4.8
		144	SMH	Store Most Half	4.8
		045	SDU	Store into Upper Byte	5.0
'	'	145	SDL	Store into Lower Byte	5.0
	Move	047	MZF	Move all Zeros Full	4.8
		147	MZH	Move all Zeros Half	4.8
		055	MIU	Move into Upper Byte	5.0
		155	MIL	Move into Lower Byte	5.0
	Exchange	056	EXF	Exchange Full	5.0
		156	EXH	Exchange Half	5.0
Transfer (Branch)	Process Register Test	062	XEF	Transfer if Process Register = 0	4.5
		162	XUF	Transfer if Process Register ≠ 0	4.5
		063	XPF	Transfer Process Register ≠ 0	4.5
		163	XNF	Transfer process Register ≠	45
	Index-,Test	064	XDO	Test, Conditionally Decrement by 1 and Transfer	4.8
		164	0XDT	Test, Conditionally Decrement by 2 and Transfer	4.8
		065	XIO	Test, Conditionally Increment by and Transfer	4.8
		165	XT	Test, Conditionally Increment by 2 and Transfer	4.8

*The direct addressing mode without indexing and the possibility of instruction-operand memory access overlap are assumed in the specification of the instruction execution times.

Table -2-1. Instructions by Classes – Continued

Instruction					Nominal execution time* (microseconds)
Class	Subclass	Function code	Mnemonic	Name	
Transfer (Branch) (continued)	Control Transfer	066	XEX	Execute	45
		060	XFR	Transfer Unconditionally	45
		160	XLK	Transfer and Store Link	4.5
		061	XSW	Transfer on Test Switches	4.5
		161	XIN	Transfer on Indicators	45
	Program Level Transfer	074	TXP	Call Executive Program Level and Link	30 To 150**
		174	TCP	Call Program Level and Link	30 To 150**
		075	TIE	Tie Program Level and Link (Semiprivileged)	30 To 150**
		133	TQR	Test and Conditionally Ret/Skip	6 To 150**
	Test Bit and Skip on Match	067	TSZ	Test Bit in Half Word for ZERO, Skip on Match	4.8
		167	TSO	Test Bit in Half Word for ONE, Skip on Match	4.8
		166	TSI	Test and Conditionally Insert/Skip	5.3
Input/Output		070	DEV	Device Command (Privileged)	6
		170	DEX	Device Command, and Exit (Privileged)	30 To 150**
		071	ITR	Input to Register (Privileged)	6
		171	OFR	Output from Register (Privileged)	6
Miscellaneous		072	HLT	Conditional Halt (Privileged)	4.5
		172	MBA	Memory Bank Assignment or Test (privileged)	10
		175	LOD	Load Call Destination (Semiprivileged)	7.1
		173	LLO	Level Lock Set (Semiprivileged)	2.9
		100	LLR	Level Lock Reset	2.9
		073	DIG	Diagnose (Privileged)	10.4
		000	NOI	No Operation Instruction	2.9
		-	TRI	Trap Instructions (Unused Codes)	2.9

*The direct addressing mode without indexing and the possibility of instruction-operand memory access overlap are assumed in the specification of the instruction execution times.

*Includes total time from instruction initiate until next instruction may be executed; since these instructions involve level changes, minimum and maximum times including level changing, are shown.

Table 2-2. Special Operand Address

Special address (Octal)	Register selected	Privileged status
000000-000037	Active Process Registers	Not Required
000040-000057	Active Page Control and Address Registers	Required
000060-000061	Privilege and Level Link Register	Required
000062, 000063	Queue Register	Required (except for TQR instruction)
000064, 000065	Query Register	Required
000066	Executive Link Register	Required
000067	Unassigned	Required
00007-000077	Program Activity Registers	Required

(h) Page designator (D), bit positions 16 through 19. This 4-bit field selects one of 16 page control and address registers as specified in para 2-5i.

(i) Word address CA), bit positions 20 through 30. These 11 bits select one of 2048 words within a page selected by the page address.

(j) Half-word address (W), bit position 31. The W-bit is used in half-word operations to select the most significant 16 bits or the least significant 16 bits of this 32-bit word as an operand. Even address (W 0) selects bits 0 through 15 of the memory word or special address register. Odd address (W 1) selects bits 16 through 31 of the memory word or special address register.

(7) Address modes. The M-field and S-field in the instruction are used to select the address mode. These modes are as follows:

(a) M=0, S=0, literal. The operand address field of the instruction is used as a 16-bit operand. No memory cycle is required to obtain an operand. It is possible to use this half word as an operand, transfer address, format instruction command, shift instruction command, or I/O command. Using this mode with fullword accumulators, the half word is assumed to be right-justified with the sign bit extended 16 bits to the left, or zero extended, depending upon the instruction type.

(b) M=0, S=1 through 7, literal with indexing. The operand address field of the instructions is used 2-10 as a 16-bit operand except, initially, the contents of the process register selected by the S-field are added algebraically to this 16-bit quantity. Overflow is detected on this addition for algebraic instructions as specified in para 2-5h.

(c) M=1, S=0, direct. The operand address field of the instruction word directly specifies an operand address. On transfer instructions, or full 32-bit operand address, W is assumed to be zero.

(d) M=1, S=1 through 7, direct with indexing. The operand address field of the instruction is added as an unsigned 16-bit quantity to the contents of the process register (index) that is selected by the S-field. Overflow on this addition is discarded and the sum is used as the new operand address, as in the direct address mode.

(e) M=2, S=0 relative The relative address mode causes the contents of the instruction location register to be added unsigned to the operand address of the instruction. Overflow in this addition is discarded and results in an operand address, relatively located with respect to the next instruction in normal sequence.

(f) M=2, S=1, relative with indexing. The operand address field of the instruction is added to the contents of process register (index) 1, and this 16-bit sum is added to the contents of the 16-bit instruction location register. This final sum is used as the operand address. Overflow on these unsigned additions is discarded.

(g) M=2, S=2 through 7, direct with double indexing. The operand address field of the instruction is added to the contents of process register (index) 01. This 16-bit sum is added to the contents of the process register (index) that is selected by the S-field of the instruction, and this final sum is used as the operand address. Overflow on these unsigned additions is discarded.

(h) M =3, S= 0, indirect The operand address field specifies a half-word location. The contents of this half-word location specify the address of the operand.

(i) M = 3, S = 1 through 7, indirect, indexed The operand address field specifies a half-word location.

The contents of this half-word location are added to the contents of the process register (index) as specified by the S-field. The sum specifies the address of the operand and overflow on this unsigned addition is discarded. The operand addresses that are generated in the nine address modes are listed in table 2-3.

e. Arithmetic Characteristics. The CPU provides the following arithmetic capabilities:
   (1) Parallel operation.
   (2) Two's complement, fixed point, integer arithmetic.
   (3) Unsigned, logical arithmetic.
   (4) Full-word and half-word operation.
   (5) Arithmetic range and value detection.

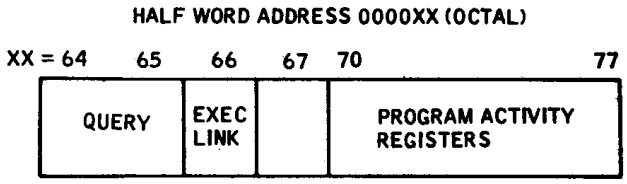
Table 2-3. Data Operand and Transfer Instruction Addresses

Instruction			Action			
M-Field (octal)	S-Field (octal)	Name	Operand address	Indirect Operand address	Operand	Transfer instruction address
0	0	Literal			CA = Z	CA = Z*
0	1-7	Literal Indexed			CA + (S)= Z	CA + (S)= Z
1	0	Direct	CA = Y		(Y) = Z	(Y) = Z*
1	1-7	Direct Indexed	CA + (S) = Y		(Y) = Z	(Y) = Z*
2	0	Relative	CA + L + 2=Y		(Y) = Z	Y = Z*
2	1	Relative Indexed	CA + L + 2 + (S = 1) = Y		(Y)= Z	Y = Z*
2	2-7	Direct Double Indexed	CA+ (S= 1)+ (S) = Y		(Y) = Z	Y = Z*
3	0	Indirect	CA = X	(X) = Y	(Y) = Z	(Y) = Z*
3	1-7	Indirect Indexed	CA = X	(X) + (S) = Y	(Y) = Z	(Y) Z*

NOTES:

CA: Instruction Address Field
L: Instruction Location
M: Mode Designator
S: Index Designator
X: Indirect Operand Address
Y: Direct Operand Address
Z: Operand
Z*: Transfer Address
( ): Contents of

f. *Program Level Characteristics.* The CPU provides for automatic switching from one program to another on a priority hierarchy through 64 program levels, and is capable of performing the following:



MS197105

Figure 2-7. Memory Address Allocation for Program Registers Common to All Program Level

(1) Detecting conditions that cause a program level change.

(2) Executing the level change by storing process registers of the current program level in allocated memory addresses, as specified in para 2-5g.

(3) Transferring the process, page control, address, and privilege and level-link registers of the new program from the allocated memory addresses (para 2-5g) to the computer's active registers.

g. *Program Registers*. A set of registers is provided for each of the 64 program levels, and meets the following general requirements:

(1) The registers for the active program level are held in the active registers of the CPU.

(2) The registers -for each of the 64 program levels are stored in fixed memory locations as specified in table 2-4, and are identified as follows:

(a) Process registers (para 2-5h).
(b) Page control and address registers (para 2-5i).
(c) Privilege and level link registers (para 2-5j).
(d) Queue register (para 2-5l).

(3) Three registers common to all program levels shall be provided with memory address allocations as specified in figure 2-7, and are identified as follows:

(a) Executive link register (para 2-5k).
(b) Query register (para 2-5m).
(c) Program activity register (para 2-5n).

h. *Process Registers*. A set of 16, 32-bit words is assigned to each of the 64 program levels and used for index registers, accumulators, and for special control. The process registers for the active program level are addressed, using the special addresses specified in para 2-5d (6). The address configuration and designators for the active process registers are shown in figure 2-8 and table 2-5. Process registers reserved for special functions are as follows:

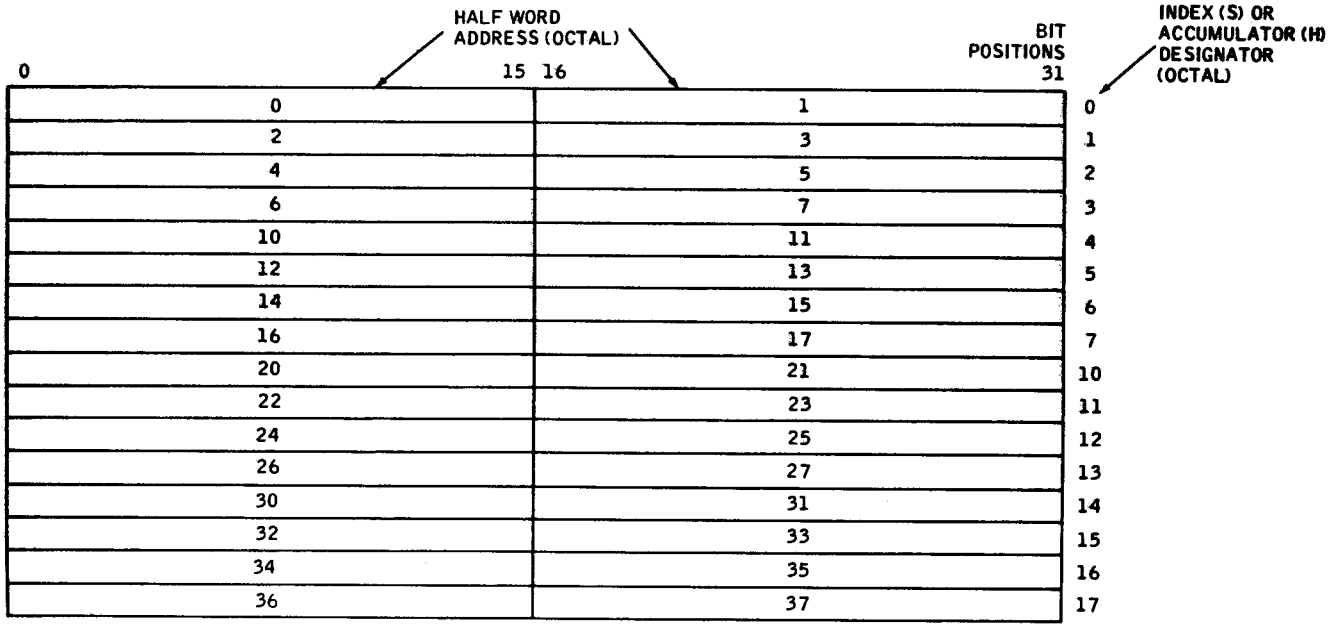


Figure 2-8. Process Register Configuration

MS 197106

Table 2-4. Allocation of Memory Address to Program Registers Unique to Each Program Level

Half-word address (octal)	Program level (octal)	Least significant bits (XX) (octal)																			
		00	01	02	03	↔	32	33	34	35	36	37	40	41	↔	56	57	60	61	62	63
0000XX	00	← Process Registers (16 X 64 Locations - 32 Bits) →											← Page Control and Address (16 X 64 Locations - 16 Bits →								
0001XX	01																	64 Privilege and Level Level Registers 32 Bits			
0002XX	02																				
0003XX	03		64 Instruction Location Registers 16 Bits						64 Mask Registers 32 Bits		64 Trap Registers 32 Bits									64 Queue Registers 32 Bits	
	64 Program Levels	64 Indicator Registers 16 Bits																			
0075XX	75																				
0076XX	76																				
0077XX	77																				

Table 2-5. Use of Process Registers

Half word address (octal)	H (octal)	S (octal)	Number of bits	Function
0			16	Indicator Register
1			16	Instruction Location Register
3		1	16	
5		2	16	
7		3	16	
11		4	16	Index Registers
13		5	16	
15		6	16	
17		7	16	
0, 1	0		32 or 16	
2, 3	1		32 or 16	
4, 5	2		32 or 16	
6, 7	3		32 or 16	
10, 11	4		32 or 16	
12, 13	5		32 or 16	
14, 15	4		32 or 16	Accumulators
16, 1'7	7		32 or 16	
20, 21	10		32 or 16	
22, 23	11		32 or 16	
24, 25	12		32 or 16	
26, 27	13		32 or 16	
30, 31	14		32 or 16	
32, 33	15		32 or 16	
34, 35	16		32 or 16	Mask Register
36, 37	17		32	Trap Instruction Register

(1) *Indicator register.* The 16 MSBs of process register 0 (half-word address 0) contain the indicators and flags for the program level. The indicator register format is shown in figure 2-9, and the functions are defined as follows:

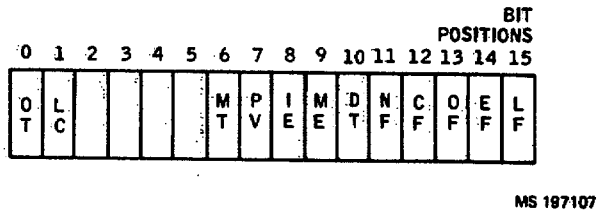


Figure 2-9. Indicator Register Format

(a) *Overflow trap override (OT), bit position 0.* If the OT bit is a zero and a fixed-point arithmetic overflow occurs, the instruction traps by executing the instruction stored in process register 17_8. If the OT bit is a one, trap on overflow does not occur.

(b) *Level change (LC), bit position 1*. The LC bit is automatically set when a program level is activated.

(c) *Memory test (MT), bit position 6.* The MT bit is set when the acceptance line on the memory communication network is not activated and has indicated an error during a memory bank assignment or test operation.

(d) *Privilege violation (PV), bit position 7*. The PV bit is set when a privileged instruction violation, special address privilege violation, memory access violation, Mode 0 excluded violation, or excluded special address violation occurs. An automatic transfer to program level 02 is also initiated.

(e) *Input parity error (IE), bit position 8.* The IE bit is reset at the start of each Input-To-Register (ITR) instruction. The IE bit is set when a parity error on the I/0 communication channel is detected during the execution of an ITR instruction.

(f) *Memory parity error(ME), bit position 9.* The ME bit is set whenever a memory-parity error is detected during a non-I/O operation. This may occur during a memory-read operation or on a memory-store operation when the quantity to be stored is less than 32 bits and the remaining word is to remain unchanged. An automatic transfer to program level 02 is also initiated.

(g) *Device timeout (DT), bit position 10*. The DT bit is reset each time an I/0 instruction is executed. The DT bit is set if the indicator signal on the I/0 communication network is not detected within the allotted 6-microsecond response period.

(h) *Nonimplemented instruction flag (NF), bit position 11*. The NF bit is set when a nonimplemented instruction code is detected. The instruction traps by executing the instruction located in process register 17_8.

(i) *Carry flag (CF), bit position 12.* The CF bit is reset at the start of an arithmetic instruction. The bit is set if there is a carryover from the MSB (sign) position in an arithmetic operation.

(j) *Overflow greater flag (OF), bit position 13*. The OF bit is reset at the start of arithmetic and compare instructions. The OF bit is set when the final result is not within the numerical range of a word. An overflow flag does not occur when a temporary overflow occurs. If the OT bit is a zero, a trap is initiated. The OF bit is also set when a compare instruction finds a greater condition, but no trap will occur.

(k) *Equal/exceed flag (EF), bit position 14*. The EF bit is reset at the start of compare instructions. The bit is set when the instruction finds an equal condition. As specified by the individual instruction, the EF bit also is set when a numerical value exceeds 16 bits (bit positions 0 through 16 are not all zeros or not all ones).

(1) *Less flag (LF)), bit position 15.* The LF bit is reset at the start of the compare instructions. The bit is set when the instruction finds a less condition.

(2) *Instruction location register*. The 16 LSBs of process register 0 (half-word address 1) contains the current instruction location for the program level. The instruction location register format is shown in figure 2-10 and the functions are defined as follows:

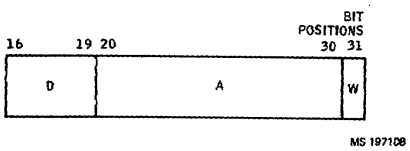


Figure 2-10. Instruction Location Register Format

(a) *Special addresses*. An address in the range 000000 to 0000378 refers to an instruction located in the process registers. An address in the range 000408 to 0000778 refers to no operation.

(b) *Page designator* (D), bit positions 16 through 19. These four bits select one of 16 page control and address registers associated with the program level. The page designation does not apply when a special address is encountered.

(c) *Word designator (A), bits 20 through 30.* These 11 bits select one of the 2048 words in a page.

(d) *Half-word designator (W9), bit 31.* This bit is ignored.

(3) *Mask register.* Process register 16_8 is the mask register that contains the information to be used in an instruction requiring a mask.

(4) *Y Trap register.* Process register 17_8 is the trap register which contains the instruction to be executed when a trap condition occurs. The trap condition occurs on an attempt to execute a nonimplemented instruction and an arithmetic overflow when the overflow trap override bit of the indicator register is a zero.

i. *Page Control and Address Registers*. A set of 16-bit half-words is assigned to each of the 64 program levels and used for determining memory access control and memory page addressing. The page control and address registers for the active program level art addressable for privileged levels using the special addresses defined in para 2-5d (6) (g). The four MSBs of the operand or instruction address, the D-field, select one of the 16-page control and address registers. The format is as shown in figure 2-11 and defined as follow.

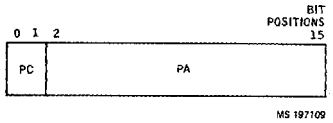


Figure 2-11. Page Control and Address Register Format

(1) *Page control (PC), bit positions 0 and 1*. Access to the memory page designated by the page address field is controlled by these two bits (table 2). When an access violation occurs, the memory is not accessed, the appropriate bits in the indicator and query registers are set, and an automatic transfer to level 02 is initiated.

Table 2-6. Page Access Control

Page access control bits	Name	Action permitted			Action inhibited		
00	Read-Write Access	Fetch Instruction	Read Operand	Write Operand	-	-	-
01	Read Access	Fetch Instruction	Read Operand	-	-	-	Write
10	Read Data Access	-	Read Operand	-	Fetch	-	Write
11	No Access	-	-	-	Fetch	Read	Write

Table 2-7. Control of the Storing and Loading of Registers in Response to an Interrupt

Bit 8	Position 9	Interrupted program level (out)	Interrupted program level (in)
0	-	Store all process registers	Load all process registers.
1	-	Store process register 0 only	Load process register 0 only
-	0	-	Load all page control and address registers
-	1	-	Load page control and address registers 0 to 3. Set page control and address registers 4 to 15 to all ONEs.

(2) *Page address (PA), bit positions 2 through 15*. The PA field addresses a unique 2048-word page of 16,384 possible memory pages. The PA field is appended to the A field of a memory reference address to form an actual 25-bit memory address. A translated address in the range 000000 to 000077_8 does not select a special address but selects a location in memory.

j. *Privilege and Level Link Register*. Each of the 64 program levels has an assigned control register that contains level link information and privilege status. These control registers are allocated to base memory bank half-word addresses 00XX60 and 00XX61 of each program level XX. Direct program modification of these addressable control words requires a privileged status. The privilege and level link word is required specifically in the execution of the call program level and link, call executive program level and link, and program level and link instruction. The word format is as shown in figure 2-12, and is defined as follows:

(1) *Privilege (P), bit potion 0 and 1.* These bits, if equal to a one-zero (10), indicate that the associated program level is permitted to execute privileged and semiprivileged instructions and access all registers represented by special addresses The associated program level is permitted to execute semiprivileged instructions when the bits are equal to zero-one (01). These bits, if equal to zero-zero (00), indicate that the associated program level is nonprivileged,

(2) *Link program level (LPL), bit positions 2 through 7.* This 6-bit field contains the number of the program level (link) that initiated the associated program level by execution of a call program level and link, call executive program level and link, or a tie program level and link instruction.

(3) *Level control (LC), bit positions 8 and 9.* When a program level change takes place in response to an interrupt, two bits control the storing and loading of registers, as specified in table 2-7. When a program level change takes place in response to a call executive program level and link instruction, or by a tie program level and link instruction, two bits shall control the loading of the registers as specified in table 2-8.

NOTE

The storing of the process registers is under control of the LC bit in the indicator register for the call program level and link, call executive program level and link, tie program level and link, and the device command and exit instruction

Table 2-8. Control of the Loading of Registers in Response to a Call Executive Program Level and Link, or Tie Program Level and Link Instruction

Bit 8	Position 9	Called executive program or tied program level
o	-	Load all process registers
1	-	Load process register 0 only
-	0	Load all page control and address registers
-	1	Load page control and address registers 0 to 3. Page control and address registers 4 to 15 are left unchanged.

(4) *Call program level (CPL), bit position 10 through 15*. This 6-bit field specifies the program level to which a transfer is called for by a call program level and link or tie program level and link instruction.

(5) *Link argument (LA), bit positions 16 through 81.* Information is communicated to a called program from the calling program by use of this 16-bit field. The half-word operand addressed in a call program level and link, call executive program level and link, or tie program level and link instruction is placed in the link argument field of the called program level's privilege and level link word. For call and tie instructions, bit 16 is tested and, if equal to zero, the status bit corresponding to the operating program level is reset. For the call program level and link instruction, bit 17 is checked and, if equal to one, program level 77_8 is stimulated. For the call program level and link instruction bit 18 is checked and, if equal to one, a bit is set in the queue register of the called program level. The bit position to be set in the queue register is specified by bit positions 19 through 23 of the A-field.

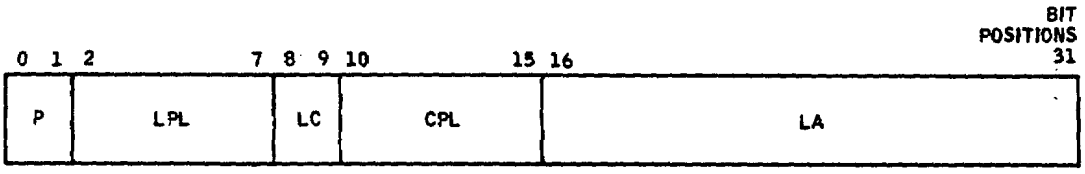


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Figure 2-12. Privilege and Level Link Register Format

k *Executive Link Register*. The executive link register contains information pertinent to program linkage with the executive program level (XPL). The register is common to all program levels and is assigned base memory bank address 000066 The register is used by the call XPL and link instruction. Program access to the addressable executive link register requires a privileged status. The half-word format is as shown in figure 2-13 and is defined as XPL, bit positions 10 through 15. This 6-bit field specifies the XPL to which a transfer is called for by a call XPL and link instruction.

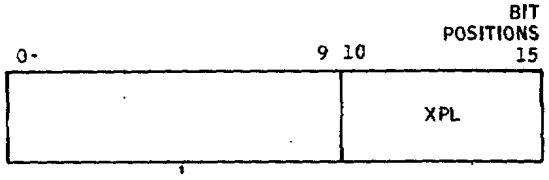

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Figure 2-13. Executive Link Register Format

I. *Queue Register*. Each of the 64 program levels has an assigned control register that contains 32 bits used in program-level communication. A bit position in the queue register is set as specified in the call program level and link instruction. A bit position is also set as specified in the termination word. A bit position is reset as specified in the test and conditionally reset skip instruction when address 62_8 is specified.

m. Query Register. The query register contains information pertaining to recognized error conditions in program execution and stipulates the currently active program level. The query register is common to all program levels and has the base memory bank addresses 000064_8 and 00006_5. Access to the query register is reserved for privileged programs. The word format is as shown in figure 2-14 and is defined as follows:

(1) *Instruction parity error (IPE), bit position 0.* The IPE bit is set when a memory parity error is detected during instruction execution. The detection occurs during instruction access, indirect address access, and operand access. The instruction experiencing the parity error is not executed.

(2) *Level change parity error (LPE), bit position 1*. The LPE bit is set when a memory parity is detected during the course of exchanging program level registers in a program level change.

(3) *Instruction violation (IV), bit position 2*. The IV bit is set when a privileged instruction violation or special address privilege violation occurs during program execution.

(4) *Memory access violation (MV), bit position 3.* The MV bit is set when a memory access violation occurs during a program execution. .

(5) *Memory timeout (MTO), bit position 4* The MTO bit is set when a memory bank has failed to respond in 60 microseconds to a memory request during program execution.

(6) *Specification violation (SV), bit position 5.* The SV bit is set when an instruction is detected for which M = 0 is excluded, or when the address refers to an excluded special address, or when an 10 instruction
is fetched in the secondary CPU.

(7) *Page designator (D), bit positions 6 through 9.* This 4-bit field designates the page control and address register related to detection of a memory parity error, access violation, or no response timeout.

(8) *Prior program level (PPL), bit positions 10 through 15.* This 6-bit field indicates the program level that experienced an error condition on the prior active program level.

(9) *Level lock indicator (LLI), bit position 16*. The LLI bit is set with the level lock set, call XPL and link, or tie program level and link instruction. The LLI bit is reset with the level lock reset, call program level and link, or device command exit instruction, and is conditionally reset with the test and conditionally reset/ skip instruction. The level lock indicator is not set by error conditions, power on, power off, or bootstrap program load.

(10) *Tentative program level (TPL), bit positions 18 through 23*. This 6-bit field indicates the program level which represents the destination program level when the trace program level is entered.

(11) Active program level (APL), bit positions 42 through 31. This 8-bit field indicates the current APL.

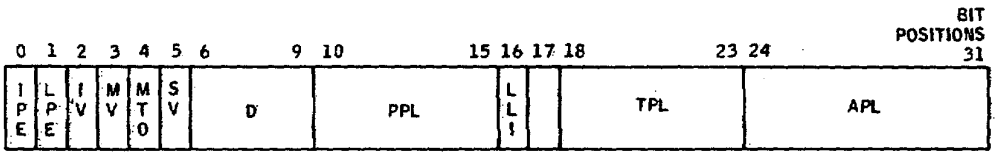

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Figure 2-14. Query Register Format

n. *Program Activity Register*. The control and status of program levels is maintained by the program activity register (PAR), which is addressable. The PAR is 128 bits and consists of eight, 16-bit half-words. Four half-words represent the program level status (PS), and four half-words represent the program level enable (PE). The contents of a pair of status-enable bits determine the operating condition for a program level as indicated in table 2-9. The bit position in the PAR is specified in table 2-10. As the table indicates, the lower the program level number, the higher the priority. Status and enable bits are set or reset by the execution of computer instructions in privileged levels only. The set and reset conditions are as follows:

(1) *Set conditions.* Status bits are set to a one as a result of any one of the following conditions:
- (a) Terminated I/0 operation.
- (b) Call program level and link instruction.
- (c) Call XPL and link instruction.
- (d) Tie program level and link instruction.
- (e) Power on (level one).
- (f) Error condition (level two).
- (g) Trace (level three).

(2) *Reset conditions.* Status bits are reset by the device command and exit instruction and conditionally reset by any one of the following:
- (a) Call program level and link instruction.
- (b) Call XPL and link instruction.
- (c) Tie program level and link instruction.
- (d) Test and conditionally reset/skip instruction.

o. *Special Program Levels.* Program levels 00 to 03 and 77_8 are reserved for special functions as follows:

(1) *Level 00 (power of).* Detection of a system or power failure causes program level 00 to be selected. The registers for the previous program level are stored in their normal memory locations. The registers corresponding to special addresses 000064_8 and 00006_5 are stored in the base memory bank at those respective locations. At the completion of these store operations, the CPU halts automatically and I/O requests are not serviced. Special address registers are not stored when a power failure occurs in program level 01.

(2) *Level 01 (automatic start).* When power is applied, the computer does not load the registers represented by special addresses 000064_8 and 000065_8 from the base memory bank, but enters and executes program level 01. I/O requests are serviced.

(3) *Level 02 (error level).* Program level 02 is automatically entered for a detected memory parity error, memory access violation, privilege violation, memory, device, or real-time clock timeout. Information available to the program includes (where applicable) the memory bank address, error type, device station address, and prior program level. I/0 requests are serviced.

Table 2-9. Program Level Operating Conditions

Situation	PS bit	PE bit	Description
Inactive	0	0	Program level is disabled and idle.
Waiting	0	1	Program level is enabled and is waiting for a response from an external equipment or another program level.
Stimulated	1	0	Equipment responded or program level was stimulated but the program level has not been enabled.
Suspended	1	1	Program level suspended because program level of higher priority is currently being executed or the program level change lock is set.
Operating	1	1	Program level is operating

Table 2-10. Address and Bit Positions for Status and Enable Bits of Program Level Activity Register

Priority	Program level number (decimal)	Program level number (octal)	Program level activity register	
			Status bits bit positions address 000070_8	Enable bits bit positions address 000071_8
Highest	0	00	0	16
	1	01	1	17
	2	02	2	18
	3	03	3	19
	4	04	4	20
	5	05	5	21
	6	06	6	22
	7	07	7	23
	8	10	8	24
	9	11	9	25
	10	12	10	26
	11	13	11	27
	12	14	12	28
	13	15	13	29
	14	16	14	30
	15	17	15	31
			000072_8	000073_8
	16	20	0	16
	17	21	1	17
	18	22	2	18
	19	23	3	19
	20	24	4	20
	21	25	S	21
	22	26	6	22
	23	27	7	23
	24	30	8	24
	25	31	9	25
	24	32	10	26
	27	33	11	27
	28	34	12	28
	29	35	13	29
	30	36	14	30
Decreasing	31	37	15	31

Table 2-10. Address and Bid Positions for Status and Enable Bits of Program Level Activity Register - Continued

Priority	Program level number (decimal)	Program level number (octal)	Program level activity register	
			Status bits bit positions address 000074_8	Enable bits bit positions address 000075_8
Decreasing	32	40	0	16
	33	41	1	17
	34	42	2	18
	35	43	3	19
	36	44	4	20
	37	45	5	21
	38	46	6	22
	39	47	7	23
	40	50	8	24
	41	51	9	25
	42	52	10	26
	43	53	11	27
	44	54	12	28
	45	55	13	29
	46	56	14	30
	47	57	15	31
			00076_8	000077_8
	48	60	0	16
	49	61	1	17
	50	62	2	18
	51	63	3	19
	52	64	4	20
	53	65	5	21
	54	66	6	22
	55	67	7	23
	56	70	8	24
	57	71	9	25
	58	72	10	26
Decreasing	59	73	11	27
	60	74	12	28
	61	75	13	29
	62	76	14	30
Lowest	63	77	15	31

(4) *Level 03 (trace level).* Program level 03 is entered automatically and temporarily when a program level change is attempted and the program level trace switch on the CTS is in the ON position. The query register contains the tentative program level that represents the destination program level. An exit from this program level does not change the PPL field in the query register.

(5) *Level 77s (bootstrap program load).* Program level 77, is entered after execution of bootstrap program load (para 2-10d(l 1)).

p. *Memory Communications Characteristics*. The CPU provides for communication with multiple memory banks as follows:

(1) *Data exchange*. All data and instruction words are stored in or received from memory as 33-bit words (of which 32 bits represent information), and one bit is such that the total number of one bit is always an odd number. Correct parity is generated for all data words prior to storage in memory. Parity is examined for all data words received from memory. The detection of a memory parity error results in the following actions:

(a) The operation is not performed.

(b) Memory is not changed.

(c) For program operations, bit 9 of the active indicator register and bit 0 of the query register are set and, during program level changes, bit I of the query register is set. The page designator is set into bits 6 through 9 of the query register.

(d) A program level change to level 02 is automatically initiated.

(2) *Addressing.* A capability of addressing 131, 072 words of 33 bits each is provided for program operations (para 2-5i).

(3) *Memory control*. When memory access conditions are satisfied (para 2-5i) for program operations, memory operations are controlled as follows:

(a) *Mode controls*. Selection of four memory modes is provided (read, read/modify, assign or test, and write).

(b) *Hold control*. This control indicates that the memory does not allow access to the other ports.

(c) *Assign or test control.* This control indicates that a memory assignment or test operation is to be performed.

q. Programmed 110 Communication Class. Four I/O instructions provided for programmed I/O communication and have the following general characteristics:

(1) They can only be executed from the CPU selected as prime.

(2) They are executed in privileged program levels only.

(3) They are executed when automatic I/O communication is not being performed or a request from device address $00\text{-}17_8$ is not pending.

(4) Their timing is independent of the peripheral device. However, an indicator signal is required within 6 microseconds of the command sequence to indicate the acceptance of the command data or that data has been transmitted. Otherwise, the device time out bit of the indicator register is set as specified in para 2-5h.

2-6. 32K Memory Unit (MU) Operation. The 32K MU (four port) forms a high-speed, high-volume assembly for storing instruction and data words used by the ADP equipment. The MU (fig. 2-15) can store up to 32, 768 33-bit words in a CMOS memory element. Access for four controllers (IOU, CPU-1, CPU-2, and DOU) is provided by the I/O bus (ports A, B, C, and D). The memory operates in four separate modes.

a. *Read.* In the read mode, a request from one of the ports is processed by the corresponding memory interface. The bank compare logic compares the bank address requested with the bank address set to make sure the correct memory bank is accessed. If they compare favorably, a request is generated to the priority port logic, which decides between simultaneous requests and applies the priority request to the timing and control logic. The timing and control logic generates a command control signal corresponding to the request, and causes the analog logic to generate a read command to the memory element. At the same time, the address register logic interprets the bank address from the data-in line and memory element to be read. The data word is read into the data register logic where it is held until transferred (by the data-out line) to the corresponding memory interface. The memory interface gates the data out to the requesting unit.

b. *Read/Modify*. In the read/modify mode, a word is read from the memory as previously described. However, the word is not read back directly into memory. Depending on the program, the data is processed by the requesting unit and the resulting modified data is read back into memory in place of the original word.

c. *Write*. In the write mode, the requesting unit's request generates a word and, through the data register logic, writes it in the memory element.

d. *Memory Bank Assignment/Test*. In the assignment/test mode, either CPU causes the addressed memory element to become active, inactive, change its bank address, or perform error checks. No information is read or written in this mode.

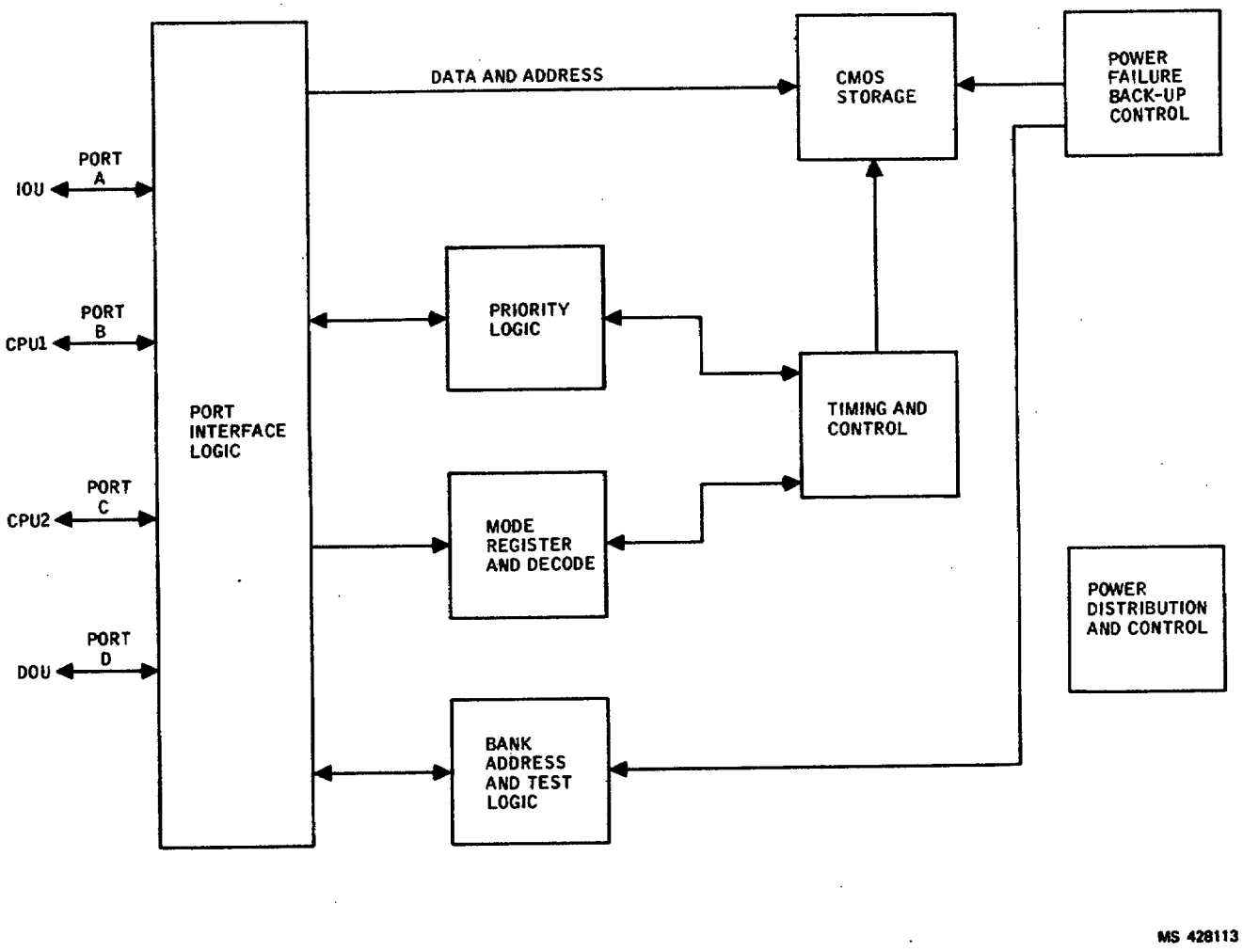

Figure 2-15. 32K Memory Unit Block Diagram

2-7. 32K Memory Unit (MU) Logic Block Description. The following paragraphs provide descriptions of the logic functions shown in figure 2-15.

a. *Port Interface Logic*. The port interface logic matches impedances, and gates and restores levels between the four independent ports and the memory logic.

b. *Priority Logic*. The priority logic determines the port to be serviced when two or more ports have requests pending at the same time. Port A has the highest priority, with B, C, and D in descending priority.

c. *Mode Register and Decode Logic*. The mode register and decode logic determines the memory cycle (read, read/modify, write or bank/assignment test) by decoding bits 0 and 1 of the information lines.

d. *Bank Address and Test Logic.* The bank address and test logic section compares the actual memory bank address (set by the front panel) against the bank address requested to determine if the request is for this bank. If so, it generates the request to the priority logic section.

e. *Timing and Control.* The timing and control section generates the command controls and timing signals necessary for memory operation.

f. *CMOS Storage*. The CMOS storage is a 32, 768 word (33-bit) RAM storage composed of 264 LSI memory devices. Each device is a 4096 X 1 CMOS chip.

g. *Power Failure Backup Control.* The backup control provides dc power from the IBDL to the CMOS RAMs to retain data storage for 30 minutes if power is shut down or fails.

h. *Power Distribution and Control.* The power distribution and control section generates and distributes the de power (+5v, -5v, and +12v) used by the memory unit.

2-8. 32K Memory Unit (MU) Detailed Description.

A detailed description of the 32K MU are given in the following paragraphs.

a. *MU Characteristics.* Each MU contains 32, 768 33-bit words (32 data bits and one odd parity bit) and provides service for four independent controllers (ports) connected to two CPUs, one IOU, and one DOU.

b. *Data Access Time*. The time required to access data in the read and read/modify modes does not exceed 600 ns after the memory bank has determined that it has been addressed.

c. *Memory Addressing*. The operand address field is the 16 high-order bits, the CA field, of the instruction word (fig. 2-6). Bits 16 thru 19 (D field) select one of 16 PCA registers (para 2-5d(6)h). The selected PCA register specifies the memory bank and page. This data is combined with bits 20 thru 30 (A field) of the instruction word (fig 2-6). The A field designates the specific address (one of 2, 048) in the bank and page specified by the PCA register. Bit 31 is not used at this time.

d. *Priority*. Access to the memory is granted to the requesting processors or controllers on a first-come, first-served basis. In the case of concurrent requests for access, port A has priority, followed by ports B, C, and D in that order. A higher priority port cannot lock out a lower priority port. Any requesting processor or controller retains access to a memory bank as long as the hold control signal is activated by the requesting unit.

e. *Memory Modes.* The 32K MU provides four modes of operation that can be selected by the unit requesting service. The four modes of operation and their associated codes are as follows:

Mode	Code number
Read (R)	00
Read/modify (RM)	01
Memory bank assignment (MBA) or test	10
Write (W)	11

(1) *Read (R) mode.* The 32K MU reads the data in the specified address, transmits the data to the requesting unit, and retains or restores the data unmodified to its former location.

(2) *Read/modify* (RM) mode. The 32K MU reads the data in the specified address and transmits the data to the requesting unit. The previously stored data is replaced by data from the unit. This new data is then stored in the same address location which was selected at the start of the cycle.

(3) *Memory bank assignment (MBA) or test*. Each 32K MU has a 3-bit MBA register that is program-changeable. The MBA word is transmitted from the CPU to the memory over the information lines.

(4) Write (W) mode. The 32K MU clears the contents of the specified address and replaces it with data from the controller.

f. *Fault Isolation Circuits*. The 32K MU is equipped with self-test circuits that can detect and isolate faults under computer control. These tests are performed in those portions of the memory where faults cannot be isolated by computer programs. For on-line fault isolation, testing is performed, on command, by internal circuits verifying proper operation of critical circuits (current sources when appropriate) which cannot be isolated by normal memory operating modes.

g. *Storage*. Data stored in the CMOS memory unit is basically volatile. However, backup control assumes data retention for 30 minutes if the power fails.

h. *Data Access*. There are no restrictions on access of data in the MU. '

i. Controls and Indicators The controls and indicators for each 32K MU, located on the ADP status and control panel, function as described in TM 9-1430-652-10-2.

2-9. Input/Output Unit (IOU) Operation. Functions of the IOU are described in the following subparagraphs.

a. *Basic Functions*. The IOU controls the transfer of data between the memory and the system's peripheral devices. These I/O operations are performed asynchronously to those of the CPU, but under the control of the CPU through the I/O commands, device keywords, and terminate words. The IOU interfaces with the peripheral devices through IOX(s) and 5 Input/Output Expanders (IOE(s)). The devices to which it is connected are as follows:

(1) I*OX1*
- 0 MTU
- 1 MTU
- 2 Radar Interface Equipment (RIE) (Report Channel)
- 3 Video Simulator Unit (VSU)
- 4 Status panel (Data Display Group)
- 5 RIE (ACP/interrupts)
- 6 Status panel (Data Display Group)
- 7 KPU

(2) *IOX2*
- 0 Display Console
- 1 Display Console
- 2-7 Spare for Display Consoles

(3) *IOX3 -Spare*

(4) *Input/output expander (IOE) 04.* Each IOE interfaces four modems to the IOU. Each modem has two addresses, with the even address assigned to the demodulator and the odd address assigned to the modulator. For example, the IOE 1 interfaces are as follows:

Modem	Addresses
5	0, 1
6	2, 3
7	4, 5
8	6, 7

b. *Additional Functions.* The IOU performs the following additional functions:
(1) Maintains 3 real-time clocks under program control. The clocks are assigned device addresses 03, 04, 05.
(2) Power sequencing for orderly start-up and shut-down.
(3) Program load (bootstrap program load).
(4) ADP status panel interface.

2-10. Input/Output Unit (IOU) Detailed Description. The IOU (fig. 2-16) controls operations between the CPU and peripheral devices and between the 32K MU and peripheral devices. The IOU contains the Input/Output Controller (IOC), Real-Time Clock (RTC), Input/Output Exchange (IOX), and Input/Output Expander (IOE), and provides logic for the ADP status and control panel.

a. *Functional Characteristics*. The IOU is functionally organized to provide the following:
(1) A queue table which permits stacking of interrupts.
(2) Memory access protection so that memory cycles cannot be initiated unless appropriate access conditions are satisfied.
(3) Parity generation and checking of memory data transfers.
(4) RTCs to generate the time of day and for control of time-dependent functions.
(5) Accept signals from the ADP status and control panel to accommodate the following:
- (a) Bootstrap program load.
- (b) Malfunction indications.
- (c) Assistance to personnel in troubleshooting.
- (d) Detection and indication of power fluctuations and power faults for both CPUs and the IOU.
- (e) Controls to conduct tests of the computer functions and peripherals, including detailed diagnostic tests.
- (f) Monitoring computer functions during normal operations.

b. *I/O Characteristics*. The IOU provides the capability for I/O functions having the following characteristics:
(1) Multiplexing data to or from 16 peripheral devices on the ac bus. Expansion capability exists for multiplexing up to 56 peripheral devices on the ac bus.
(2) Multiplexing of an additional 64 devices over a common multiplexing device.

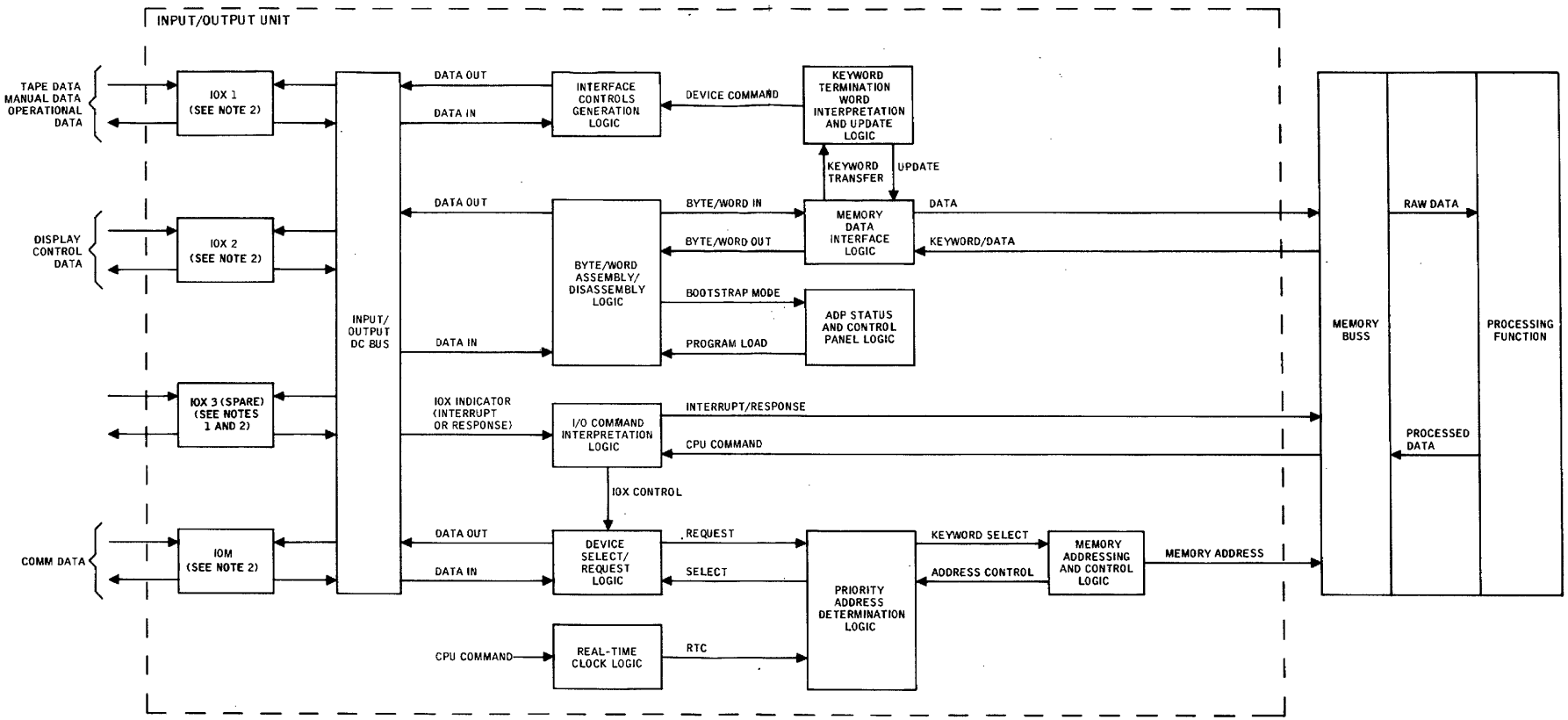

Figure 2-16. Input/Output Unit (IOU) Block Diagram

(3) Bidirectional direct data transfers with multiple peripheral devices located at distances up to 150 meters, concurrent with instruction execution.

(4) Priorities for servicing of data transfer operations with peripheral devices.

(5) Data transfer fault detection.

c. *Memory Communication Characteristics*. The IOU provides for communication with multiple memory banks as follows:

(1) *Information exchange*. The IOU provides an independent communication network for communicating with the multiple memory banks for automatic I/O operations. Information exchange includes data, address, and control functions.

(2) *Data exchange*. All data and control words are stored in (or received from) memory as 33-bit words (32 bits represent information and one bit is the parity bit). The number of one bits is always an odd number. Correct parity is generated for all words prior to storage in memory. Parity is examined for all words received from memory. The detection of a memory parity error results in the following:

(a) The operation is not performed.

(b) The memory is not changed.

(c) For automatic I/O operations, bit 11 or bit 12 of the monitor register is set. The addressed memory bank number is set into bits 21 through 24 of the monitor register. The device address is set into bits 25 through 31 of monitor register.

(d) A program level change to level 02 is automatically initiated.

(3) *Addressing.* Up to 131, 072 words of 33 bits each can be addressed in automatic I/O operations.

(4) *Memory control* When memory access conditions are satisfied, memory operations for automatic 110 operation are controlled as follows:

(a) *Mode controls.* Selection of one of the four memory modes (described in para 2-6) is provided.

(b) *Hold control.* The hold control indicates that the memory allows no access to the other ports.

d. *I/O Data Communication*. The computer provides control for data communications with peripheral devices having programmed I/O operations, and with those having automatic I/O communications independent of instruction execution.

(1) *Programmed I/O communication class*. The I/O instructions provide for programmed I/O communications, and have the following general characteristics:

NOTE

Since these instructions are possible only when the IOU and CPU are connected together, the functions performed by both units are included.

(a) Accepted only from the CPU designated primary.

(b) Executed only in privileged program levels.

(c) Executed when automatic I/O communication is not being performed or a request from device address $00\text{-}17_8$ is not pending.

(d) Have timing that is independent of the peripheral device. However, an indicator signal is required within 6 microseconds of the command sequence to indicate the acceptance of the command data or that data has been transmitted.

(2) *Programmed I/O operations*. The I/O instructions operate as follows:

(a) *Device command (DEV*). Execution of the CPU DEV command causes the eight MSB positions (bit positions 16 through 23) of the instruction operand (fig. 2-17) to be transmitted to the peripheral device addressed by the eight LSB positions (bits 24 through 31) of the operand. Only peripheral device addresses 000 through 177 are used. The H field of the instruction word is not used. All modes of address modifications as specified by the M field are allowed.

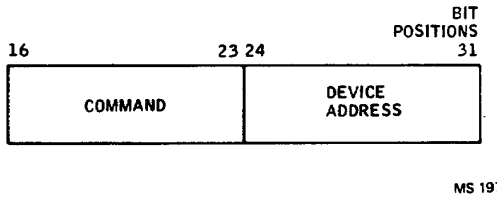

Figure 2-17. Device Command and Device Command and Exit Instruction Operand Format

(b) *Device command and exit (DEX*). The DEX instruction operates as described in para 2-10d(2) (a) with the following additions: the instruction causes the status bit in the program activity register corresponding to the operating program level to be reset; and the level change lock flip-flop is reset and a program level change occurs.

(c) *ITR*. The CPU ITR instruction causes the peripheral device addressed by the eight LSB positions of the instruction operand (fig. 2-18) to transmit one to four 8-bit bytes to the IOU. Only peripheral device addresses 000 thru 177_8 are used. The transmitted data is stored in the process register specified by the H field of the instruction. All address modes are allowed. The

parity is checked and, if correct, the input parity error bit in the indicator is reset. Incorrect parity sets the indicator bit as specified in para 2-5h.

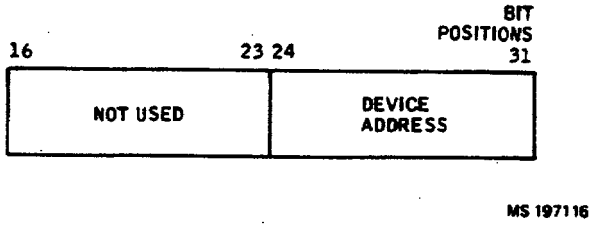

Figure 2-18. Input-To-Register and Output-From-Register Instruction Operand Format

(d) *Output-from-register (OFR).* The CPU OFR instruction causes the eight LSB positions of the instruction operand to select the peripheral device. Only peripheral device addresses 000 through 17_8 are used. The contents of the process register, addressed by the H field of the instruction word, are transmitted to the device as four 8-bit bytes. All modes of address modification are allowed.

(e) *Special I/O commands*. The special I/O commands operate as follows: DEV address 00 with bit 16 of the command byte set causes the IOU to send a level interrupt signal to the secondary CPU. OFR address 00 causes the IOU to load the memory access violation matrix as indicated in table 2-11. ITR address 01 causes the IOU to place the contents of the monitor register on the CPU to IOU bus. OFR address 01 causes the IOU to set each bit of monitor register as specified by a one in the OFR data word. Zero bits in the OFR data word have no effect on the monitor register bits. ITR address 02 causes the IOU to place the status of the ADP status and control panel (table 2-12) on the IOU to CPU bus. OFR address 02 causes the IOU to reset each bit of the monitor register as specified by a one in the OFR data word. Zero bits in the data word have no effect on the monitor register. DEV address 03 causes the IOU to command the RTCs as specified in para 2-10g. DEV address 00 with bit 17 of the command byte set causes the IOU to send a start signal to the secondary CPU.

Table 2-11. Input/Output Memory Access Control Fields for Output-From-Register (OFR) Instruction to Device-Address

Memory bank address (octal)	Bit position									
	16	17	18	19	20 23	24 25	26 27	28 29	30 31
00	0	0	0	0	Not Used	Access	Access	Access	Access
01	0	0	0	1					
02	0	0	1	0		Control	Control	Control	Control
03	0	0	1	1					
04	0	1	0	0		Bits	Bits	Bits	Bits
05	0	1	0	1					
06	0	1	1	0		for	for	for	for
07	0	1	1	1					
10	1	0	0	0		First	Second	Third	Fourth
11	1	0	0	1					
12	1	0	1	0		Page	Page	Page	Page
13	1	0	1	1					
14	1	1	0	0		of	of	of	of
15	1	1	0	1					
16	1	1	1	0		2048	2048	2048	2048
17	1	1	1	1					
						Words	Words	Words	Words

Table 2-12. Input-To-Register (ITR) Device Address 02

Bit position	Indicator switch signal	Remarks
0-2	Not Used	
3	Environmental Signal	"0" one of the environmental errors exists
4	Voice Comm. Central Panel Signal	"0" fault condition in voice comm. central exists
5	Main Power Signal	"0" main power fault
6	PRIMARY CPU SELECT Toggle Switch	"0" lower CPU = Primary "1" upper CPU = Primary
7-9	Not Used	
10	IOX-1 Toggle Switch	1 = On Line; 0 = Off Line
11	IOX-2 Toggle Switch	1 = On Line; 0 = Off Line
12	IOX-3 Toggle Switch	1 = On Line; 0 = Off Line
13	IOM Toggle Switch	1 = On Line; 0 = Off Line
14	Keyboard Printer	1 = On Line; 0 = Off Line
15	Not Used	
16-21	PROGRAM/TEST Thumbwheels Switch	Bits 16-18 associated with most significant thumbwheel bits 19-21 associated with least significant thumbwheel (64 selections)
22-24	Not Used	Not used in AN/TSQ-73
25-31	Not Used	Not used in AN/TSQ-73

(3) *Automatic I/O communication.* Automatic I/O communication is controlled by the contents of two control words (keyword and termination word). There are 126 keywords and 126 termination words stored in reserved locations of the base memory bank, as shown in table 2-13. Each pair corresponds to a device address. Device addresses 00 through 07 are reserved for special computer functions as shown in table 2-13. Extended device addresses 10 through are used with an Input/Output Multiplexer (IOM). Automatic I/0 communication is independent of program execution. A program interrupt is initiated at termination of a block transmission or receipt of a device interrupt. The control words are described in the following paragraphs.

(4) *Keyword* The keyword contains three fields (fig. 2-19) to specify the block length (in words or bytes) of the transmission, I/O mode of communication, and current data memory address as follows:

(a) *Block length (BL), bit positions 0 through 10.* This 11-bit field specifies either the number of words or number of bytes in a block data transmission, or the number of time events in the alarm (clock) mode. A zero block length indicates the maximum block length of 2048 words, bytes, or events. Blocks larger than 2048 are obtained under control of the peripheral device. For each data transfer or time event, the block-length field is decremented. When this field is decremented to zero, the block transmission is terminated if the channel end bit in the termination word so specifies, or if the device initiates a device interrupt sequence after receiving the End-Of-Block (EOB) command.

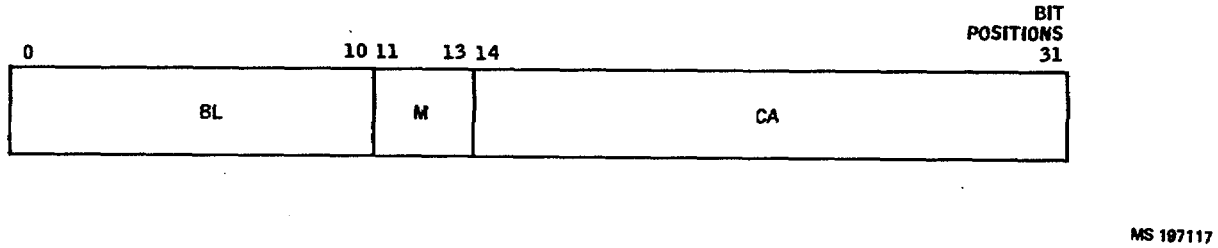

Figure 2-19. Input/Output Keyword Format

Table 2-13. Automatic Input/Output Control Words

Memory address (octal)	Least significant memory address digits (XX) (octal)								
	70	71	72	73	74	75	76	77	
0000XX	Not Available				Not Available				
0001XX	ADP Panel Interrupt (START)				Device Address 03 (RTC 0)				
0002XX	Device Address 04 (RTC 1)				Device Address 05 (RTC 2)				
0003XX	Device Address 06 (Not Used)				Device Address 07 (Not Used)				
0004XX	Device Address 10				Device Address 11				
0005XX	Device Address 12				Device Address 13				
0006XX	Device Address 14				Device Address 15				
0007XX	Device Address 16				Device Address 17				
0010XX	Device Address 20				Device Address 21				
0011XX	Device Address 22				Device Address 23				
↓	↓				↓				
0027XX	Device Address 56				Device Address 57				
0030XX	Device Address 60				Device Address 61				
0031XX	Device Address 62				Device Address 63				
0032XX	Device Address 64				Device Address 65				
0033XX	Device Address 66				Device Address 67				
0034XX	Device Address 70				Device Address 71				Priority Increases
0035XX	Device Address 72				Device Address 73				
0036XX	Device Address 74				Device Address 75				
0037XX	Device Address 76				Device Address 77				
0040XX	Device Address 100				Device Address 101				
0041XX	Device Address 102				Device Address 103				
0042XX	Device Address 104				Device Address 105				
0043XX	Device Address 106				Device Address 107				
0044XX	Device Address 110				Device Address 111				
0045XX	Device Address 112				Device Address 113				
0046XX	Device Address 114				Device Address 115				
0047XX	Device Address 116				Device Address 117				
0050XX	Device Address 120				Device Address 121				
0051XX	Device Address 122				Device Address 123				
↓	↓				↓				
0067XX	Device Address 156				Device Address 157				
0070XX	Device Address 160				Device Address 161				
0071XX	Device Address 162				Device Address 163				
0072XX	Device Address 164				Device Address 165				
0073XX	Device Address 166				Device Address 167				
0074XX	Device Address 170				Device Address 171				
0075XX	Device Address 172				Device Address 173				
0076XX	Device Address 174				Device Address 175				
0077XX	Device Address 176				Device Address 177				
	Keywords		Termination Words		Keywords				Termination Words

(b) Mode (M), bit positions 11 through 13. This 3-bit field is as specified in para 2-10d(6), and describes one of the following modes of operation:

M = 0 Inactive
M = 1 Output, full word by bytes
M = 2 Alarm (clock)
M-= 3 Input, full word by bytes
M = 4 Output, upper byte in half word
M = 5 Output, lower byte in half word
M = 6 Input, upper byte in half word
M = 7 Input, lower byte in half word

(c) Current address (CA), bit positions 14 through 31. This 18-bit field specifies directly the halfword address of the memory location related to the current data transfer. For 32-bit word-by-bytes transfers, the least significant bit (LSB) is ignored. The field is incremented as defined in para 2-10d (6).

(5) Termination word The termination word is used to indicate conditions of transmission and to specify the program level to be stimulated at termination of a block data transmission or receipt of a device interrupt. The format of the termination word is as shown in figure 2-20. The fields are described as follows:

(a) Block complete (F), bit 0. The F-bit is set if the associated keyword has been decremented from one to zero.

(b) Interrupt (I), bit 1. The I-bit is set when an interrupt is received from a peripheral device. The indicator signal represents a device interrupt.

(c) Normal program level (NPL), bits 2 through 7. This 6-bit field defines the program level to be stimulated if the F-bit or I-bit of the termination word is set and the transmission error (E) and operational error (R) bits are zero.

(d) E, bit 8. The E-bit is set when the computer detects a parity error on the I/O communication network during an automatic data transfer operation.

(e) R, bit 9. The R-bit is set if a request for service is received from a device and inactive mode 0 is stipulated in the keyword, a memory parity error occurs during access of keyword or data word, or a memory access violation occurs as defined in para 2- 10d(12).

(f) Error program level (EPL), bits 10 through 15. This 6-bit field defines the program level to be stimulated if the F- or I-bit and E-bit is set and the R-bit is zero.

(g) Channel end (C), bit 16. The presence of the C-bit causes immediate termination and interrupt on depletion of the block length. Absence of the C-bit specifies a device-end termination and interrupt that does not occur until the device initiates a device-interrupt sequence.

(h) Parity terminate (P), bit 17. The presence of the P-bit causes the termination program level to be stimulated when a parity error is detected on the information lines in the automatic input mode.

(i) Queue table (Q), bits 18 through 23. When bit position 18 contains a zero, bit positions 19 through 23 are ignored and no action takes place. When bit position 18 contains a one, bit positions 19 through 23 cause a bit to be set in the queue register corresponding to the termination program level. The bit position in the queue table is specified by bit positions 19 through 23. This action takes place only when a termination program level is stimulated.

(j) Device status (D), bits 24 through 31. The data on the information lines during a device interrupt sequence is stored in bit positions 24 through 31.

(6) Modes of operation The M field of the I/O keywords determines the mode of control that the IOU executes when it processes a request from a peripheral device, as follows:

(a) M = 0, inactive mode If the IOU detects that the mode field contains in the keyword all zeros, the IOU sets the R-bit of the corresponding termination word, issues a stop sequence to the device, and initiates a program level change to level 02.

(b) M = 2, alarm (clock) mode In the alarm mode, the BL field of the keyword is decremented by one each time a request from an external source is serviced. The CA field is not modified and no data transmission occurs.

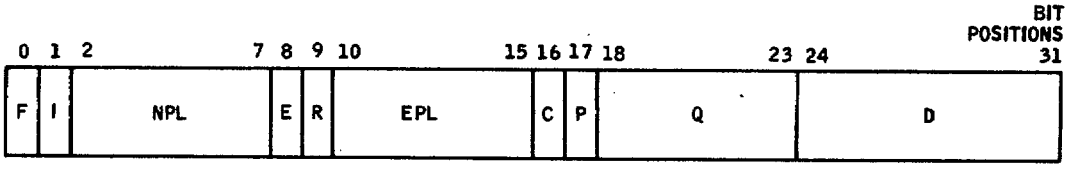

Figure 2-20. Input/Output Termination Word Format

(c) M = 1 or 3, full-word output or input The modes are for the transmission of full 32-bit words, which are transmitted as four bytes plus parity. The BL field is decremented by one for each word transmitted or received. The CA field is incremented by two for each word transferred.

(d) M = 4 or 6, upper byte in half-word output or input. Data is transmitted or received as bytes (8 bits plus parity). The data is unpacked from the eight MSBs in a 16-bit half word on output and packed into the eight MSBs in a 16-bit half word on input as addressed by the CA field. The CA field is not changed. The M field is automatically changed from 4 to 5 or 6 to 7, so that the next byte transmitted is the lower byte. The BL field is decremented by one.

(e) M = 5 or 7, lower byte in half-word output or input . Data is transmitted or received as bytes (8 bits plus parity). This data is unpacked from the eight LSBs in a 16-bit half word on output and packed into the eight LSBs in a 16-bit half word on input as addressed by the CA field. The CA field is incremented by one and the M field is automatically changed from 5 to 4 or 7 to 6, so that the next byte transmitted is the upper byte. The BL field is decremented by one.

(7) Types of operation. The IOU communicates with external devices in blocks of words by bytes or byte transmission, alarm operation, device interrupt, and bootstrap program load, as described in the following paragraphs.

(8) Block transmission. Block transmission between the IOU and peripheral devices has the following characteristics:

(a) A DEV or DEX instruction signals the interface buffer of a peripheral device to transmit or receive data. The program-loaded keyword determines the block length and data memory address.

(b) The IOU accepts a request-for-service signal to transfer data.

(c) On acknowledgment of the request, the proper keyword is obtained from memory. The keyword is modified as specified in para 2-10d(6) and returned to memory, and the word or byte is transferred within 6 microseconds, provided that the associated memory banks are not being used for programmed operations.

(d) When the BL field is decremented from 1 to 0, the termination word is accessed, the F-bit is set, and an EOB command sequence is sent to the device. Termination occurs if the channel-end bit is present or if the device responds with a device interrupt sequence.

(e) When a termination occurs, the program level specified by the NPL field is stimulated unless the E-bit has been previously set.

(f) Abnormal conditions occurring during the data transfer are indicated in the monitor register and displayed on the ADP status and control panel as specified in para 2-10a. They include the following: (1) The E-bit of the termination word is set when the computer detects a parity error on the I/O network during data transfer (data transfer continued); (2) the R-bit of the termination word is set, an interrupt to program level 02 occurs, and the computer transmits a stop sequence to the device if a response to an enable signal is not received within 6 microseconds; (3) a memory parity error is detected in data or keyword access or a violation of memory access occurs; and (4) detection of a parity error during access of the termination word causes a transfer to program level 02, and the termination word remains unmodified. Also included in such abnormal conditions is a request for service on a channel with an inactive keyword.

(9) Alarm (clock) operation. The alarm operation is as specified for block transmission except that data is not transmitted and the CA field is not used.

(10) Device interrupt. When the computer acknowledges a request for service and the indicator signal is active, the following actions occur: (1) The I-bit of the termination word is set; (2) the program level specified by the NPL field is stimulated if the E-bit and R-bit are zero; and (3) the program level specified by the EPL field is stimulated if the E-bit is a one.

(11) Bootstrap program load. A bootstrap load operation is initiated from a switch setting on the ADP status and control panel as specified in para 2-10e, and the IOU executes the following: (1) Resets and inhibits the RTCs; (2) transmits a special device command (bootstrap) to the device with address 10_8 or 11_8; (3) generates a keyword from the first seven bytes received; and (4) inputs data under control of the keyword. It also transfers to program level 77_8 when the block length has been decremented to zero, indicating termination of transfer, and executes the instructions in program level 77_8.

(12) I/O memory access control The I/O memory access control applies to memory data transfers associated with automatic I/O communications as follows:

(a) I/O memory access control is defined by two control bits for each of the 64, 2048-word pages within the memory addressing capability associated with automatic I/0 communications. The two bits control memory access as indicated in table 2-14. When the access violation occurs, the computer does not access the memory, but sets the appropriate bits in the monitor register defined in para 2-10e(2), and initiates a transfer to program level 02. The computer has read and write access to the keyword and termination word, regardless of the access control bit configuration for the related portion of memory.

(b) OFR instructions to special device address 00 establish the memory access control. The least-significant 16 bits of the selected accumulator define the memory access for each 2048-word page of the 32K word memory bank shown in table 2-11. The remaining bits are unused.

e. *Controls and Indicators.* The controls and indicators associated with the IOU are located on the ADP status and control panel, which is integral to the computer and program (refer to TM 9-1430-652-10-2). The IOU controls and indicators are as described in the following subparagraphs.

(1) Diagnose status indication. The IOU has built-in error detection and isolation capabilities. This self-test feature functions automatically when the operator selects either CHANNEL 10 or CHANNEL 11 on the ADP status and control panel. The diagnose indicators indicate the self-test status to the operator.

(2) System status indication. The IOU contains a 32-bit monitor register with information content as listed in table 2-15. The conditions for controlling the bits of the register are as specified in table 2-11. All bits of the register are program controllable and are accessible by the CPU as follows:

(a) An OFR command to device address 01 sets the bits in the monitor register. A one in a bit position of the OFR address sets the corresponding bit of the register to a one. A zero has no effect on the corresponding register bit.

(b) An OFR command to device address 02 resets the bits in the monitor register. A one, in a particular bit position of the OFR, resets the corresponding bit of the register to a zero. A zero has no effect on the corresponding bit.

(c) An ITR command to device address 01 causes the contents of the monitor register to be transferred to the process register specified by the H field of the instruction.

(3) Maintenance and fault isolation . The ADP status and control panel contains the required controls and indicators to assist in fault isolation and maintenance functions during bootstrap program load operations and during power-on sequencing. Hardware monitors decode conditions that occur during these operations. The format of the ITR device address 02 is shown in table 2-12.

(4) Power on-off sequence and monitor. A power on-off sequence detects a prime power failure, initiates a shut-down sequence, detects the restoration of power, initiates a start-up sequence, and provides proper sequencing of logic and power signals to the processors and memories. This provides an orderly shutdown and start-up of the computer with the preservation of memory information during these periods. The start-up and shut-down sequences operate as follows:

(a) Start-up sequence. When the prime power is applied, a delay is required to allow the voltage regulators to reach full output voltage. At this time, the master reset and memory inhibit signals are removed and the computer start signal is activated. The start-up sequence is not initiated unless the shut-down sequence has already been completed and the MASTER RESET control has been activated.

(b) Shut-down sequence. A voltage detector senses when the prime power is removed (either by turn-off or as a result of a power failure). The power removal results in a device drive inhibit signal being sent to the computer and causes an internal interrupt. After at least a 125-microsecond delay (to provide time for the hardware storage operation to take place in the computer), the memory inhibit signal is applied to protect the memory. This is followed by activation of the MASTER RESET control, which remains activated during down-time. Once initiated, the shut-down sequences to completion even if the voltage is restored.

Table 2-14. Input/Output Memory Access Control

I/O memory access control bits	Name	Action permitted		Action inhibited	
00	All Access	Read	Write	-	-
01	Output Only	Read	-	-	Write
10	Input Only	-	Write	Read*	-
11	No Access	-	-	Read	Write

*A read operation for the purpose of inserting a byte in a memory cell shall be allowed with this control configuration.

Table 2-15. Input/Output Unit Monitor Register

BIT	Function/Indicator
00	Not Used
01	IOU Fault Indicator (ADP Status and Control Panel)
02	PRIME CPU Fault Indicator (ADP Status and Control Panel)
03	PROGRAM LOAD (Channel 11) Indicator (ADP Status and Control Panel)
04	PROGRAM LOAD (Channel 10) Indicator (ADP Status and Control Panel)
05	START Test Indicator (ADP Status and Control Panel). Pressing this switch causes an interrupt
06	SEC CPU Fault Indicator (ADP Status and Control Panel)
07	Not Used
08	Device Input Parity Error (Set by IOU)
09	Device Response Time-out - 6 Microseconds (Device Hung-up)
10	I/O Memory Protect Violation (Set by IOU)
11	I/O Memory Parity Error on Control Word (Set by IOU)
12	I/O Memory Parity Error on Data Word (Set by IOU)
13	Memory Time-out - 60 Microseconds (Set by IOU)
14	IOC Time-out - 250 Microseconds (IOC failed to honor real-time clock request)
15	Program Time-out (Set by IOC) - Set when the keyword block length field for real-time clock (device address 03) is not reinitialized within 980 microseconds after it has decremented to ZERO
16 to 20	(To be defined by the program)
21 to 24	Memory bank address when I/O parity error or privilege violation occurs, or timeout (bit 21 is ZERO, bit 22 is MSB of memory address)
25 to 31	Device address when any device error occurs (bit 25 is ZERO, bit 26 is MSB of device address)

f. RTC. The RTCs are a function of hardware interval timers and programmed counters which operate in the alarm mode as follows:

(1) Device addresses 03, 04, and 05 are assigned to the RTCs.

(2) When activated, the RTCs initiate service requests at intervals of 1024 ± 02 microseconds.

(3) When the BL field of the keyword for device address 03 is decremented to zero, the M field is set to zero.

(4) If an RTC issues a request for service when the M field is zero, a program hang-up condition occurs and is indicated by:

(a) The setting of the R-bit of the associated termination word.

(b) The setting of bit 15 of the monitor register and automatic transfer program level 02.

g. RTC On/Off Control. RTCs 0, 1, and 2 are assigned device addresses 3, 4, and 5, respectively. The RTCs are deactivated when a bootstrap is initiated or the power is turned off. Activation of the RTCs is under program control. A device command (DEV or DEX), with device address 03, determines whether any or all of the RTCs are active. After an RTC is activated, the first request for service occurs between 1 and 1024 microseconds. The format of the instruction operand is as shown in figure 2-21. The fields are as follows:

(1) On control bits 16, 17, and 18 control the activation of RTCs 0, 1, and 2. If the bit is a one, the RTC. is activated. If the bit is a zero, the RTC ignores the bit.

(2) Off control bits 20, 21, and 22 control the deactivation of RTCs 0, 1, and 2. If the bit is a one, the RTC. is deactivated. If the bit is a zero, the RTC ignores the bit.

(3) Device address, bits 24 to 31 are set to 003_8.

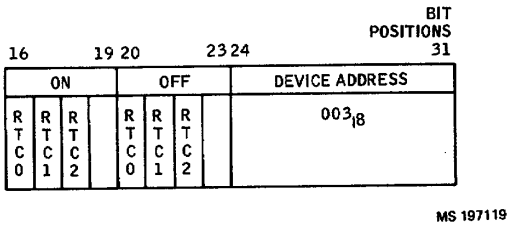

Figure 2-21. Real Time Clock Activity Command Control Format

h. Input/Output Exchange and Input/Output Expander (IOX/IOU) Networks. Each IOX/IOU network provides the following:

(*1)* Acceptance of service requests for up to eight peripheral devices on its I/O communication channel.

(2) Indication to the computer of devices requesting service.

(3) Transfer of requests and data from the peripheral devices on the I/O communication channel to the computer over the dc communication bus.

(4) Recognition and interpretation of addresses intended for devices on its I/O communication channel and selection of the designated device.

(5) Transfer of commands and data to an addressed device on its I/O communication channel.

(6) Provisions to inhibit a request to the IOU by a switch located on the ADP status and control panel. Activation of these switches places all devices on the switched IOX to an off-line position.

(7) Determination of the most significant octal digit of the device address associated with the devices of a particular I/O communication channel by uniquely wiring the channel select and request lines for each IOX/IOU.

(8) Recognition of computer-generated master resets (command and enable lines), and reset of IOX/IOU request register.

2-11. Buffer Unit Operation. The buffer unit contains the logic for the IOX/IOUs, Display Output Unit (DUO), and Keyboard Printer Unit (KPU). The buffer unit comprises two IOUs, with wiring for a third, and five IOUs, with wiring for three more. Each IOX or IOU has the ability to interface with up to eight devices to the IOU. The only difference between an IOX and an IOU is in the electrical drive capability. An IOX can interface with devices at distances up to 150 meters. The IOUs can service devices at distances of up to 50 meters away. The DOU interfaces the display consoles directly with the memory. The DOU initiates a memory request approximately every 8 microseconds, and transmits a word down the display bus for every console to evaluate. The DOU removes the display console updating from the I/O data load on the IOU. A block diagram of the DOU is shown in figure 2-22. The DOU interfaces with both the memory and display consoles. The characteristics of each interface are as follows:

a. DOU Memory Communication Interface. The memory communication interface has the following features:

(1) It is capable of addressing 32K memory addresses. If an End-Of-File (EOF) is not received before the DOU has addressed 32K memory addresses, the address register resets to 0000 and the sequence continues from this address.

(2) It enables a 60-microsecond timer on each memory cycle to detect a memory timeout. If the time elapses, a memory timeout fault exists.

(3) It only uses the read mode in memory access.

(4) It checks for parity on all memory data. The memory parity fault exists when a parity check error is detected.

(5) It obtains the starting address of the display refresh file from bank 0. Address 0000 of the 32K memory bank 0 contains the DOU control word (fig. 2-23).

(6) It continues to output data when a memory parity error is detected on a data word.

(7) It inhibits the output of data when a memory parity error is detected on a control word.

b. DOU Console Communication Interface. The console communication interface has the following features:

(1) It transforms the memory data into 4 data bytes and outputs on the display interface.

(2) It sends a sync signal with the first data byte of each word.

(3) When an all-zero control field in the control word is detected, it continues requesting memory services until a control word with a nonzero control field is received.

(4) It is capable of interfacing with display consoles at distances up to 100 meters.

(5) It transforms the 32-word memory word into a word-by-byte format and applies the result to the display interface.

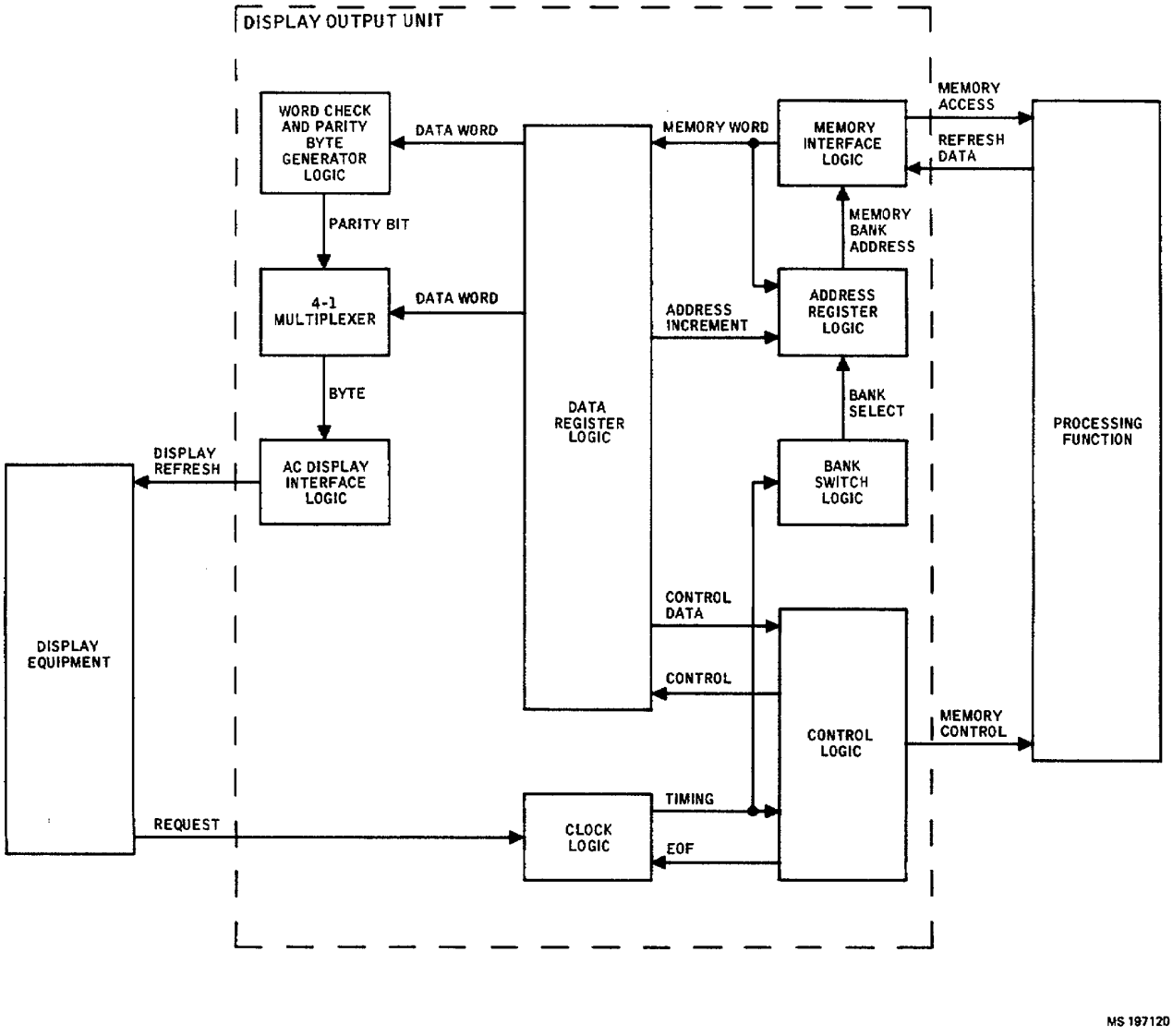

Figure 2-22. Displaying Output Unit Block Diagram

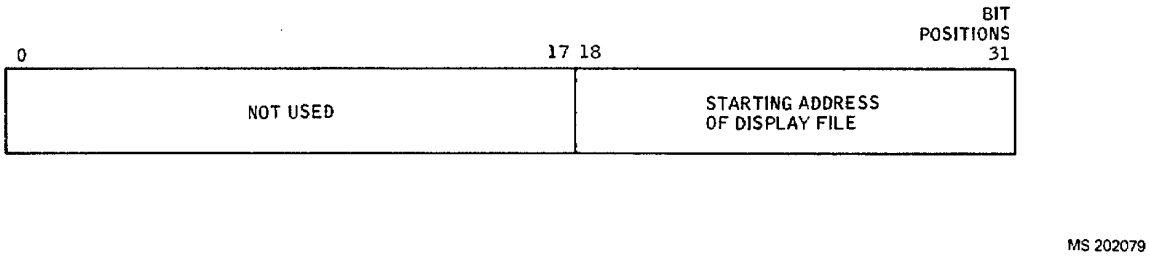

Figure 2-23. Control Word for Display Address

c. DOU Fault Condition Characteristics. The DOU fault condition characteristics are as follows:

(1) When a control word parity error or memory timeout occurs, the DOU does not resume operation until a master reset and start or restart signal is received from the ADP status and control panel.

(2) When EOF is detected, the DOU enters a wait state until the 50-microsecond timer elapses.

(3) The DOU enters the active state when the 50-microsecond timer elapses if an EOF has been received and the request-inhibit line is false. When the 50-microsecond timer elapses and EOF has not been detected, an overrun fault exists. When the overrun fault is detected, operation continues in a normal manner.

d. DOU Master Reset Operation. When a master reset signal is received, the master reset operation returns the DOU to the idle state, resets all logic, and awaits a start signal from the commanded display console.

e. DOU Initiate Operation. The DOU initiate operation recognizes a start signal from the commanded display console to initiate data exchange between a selected 32K MU and display interface (active state). It activates the 50-microsecond timer when a start signal is detected. It accesses, in the active state, the selected 32K MU beginning with address 0000 at a 5.5 microsecond rate until EOF is detected in the data field or the master reset signal is detected on the display interface.

2-12. Keyboard Printer Unit (KPU) Operation. The KPU is a peripheral device which allows the operator to communicate with the computer, and has 40-character/second output rate. The system software normally maintains the unit in the input mode (to computer) unless the computer has a message to be output. An indicator on the KPU lights to indicate that it is in the input mode. A block diagram of the KPU controller is shown in figure 2-24. The KPU performs the following functions: (1) transmits operator-initiated data to the computer; (2) transmits computer-initiated data to the printer; (3) self-test; (4) creation of a printed record of the input or output (not test) transactions; and (5) creation of a printed record when off-line. Detailed KPU operations are described in the following paragraphs.

NOTE

In addition to use of the KPU to communicate with the computer, the AN keyboard on the Display Console panel can be used to enter data into the computer (through the display console) for execution of various control commands and exercise of certain software programs. More complete data on theory and maintenance of the AN keyboard is contained in the Display Equipment maintenance manual TM 9-1430-655-20-4.

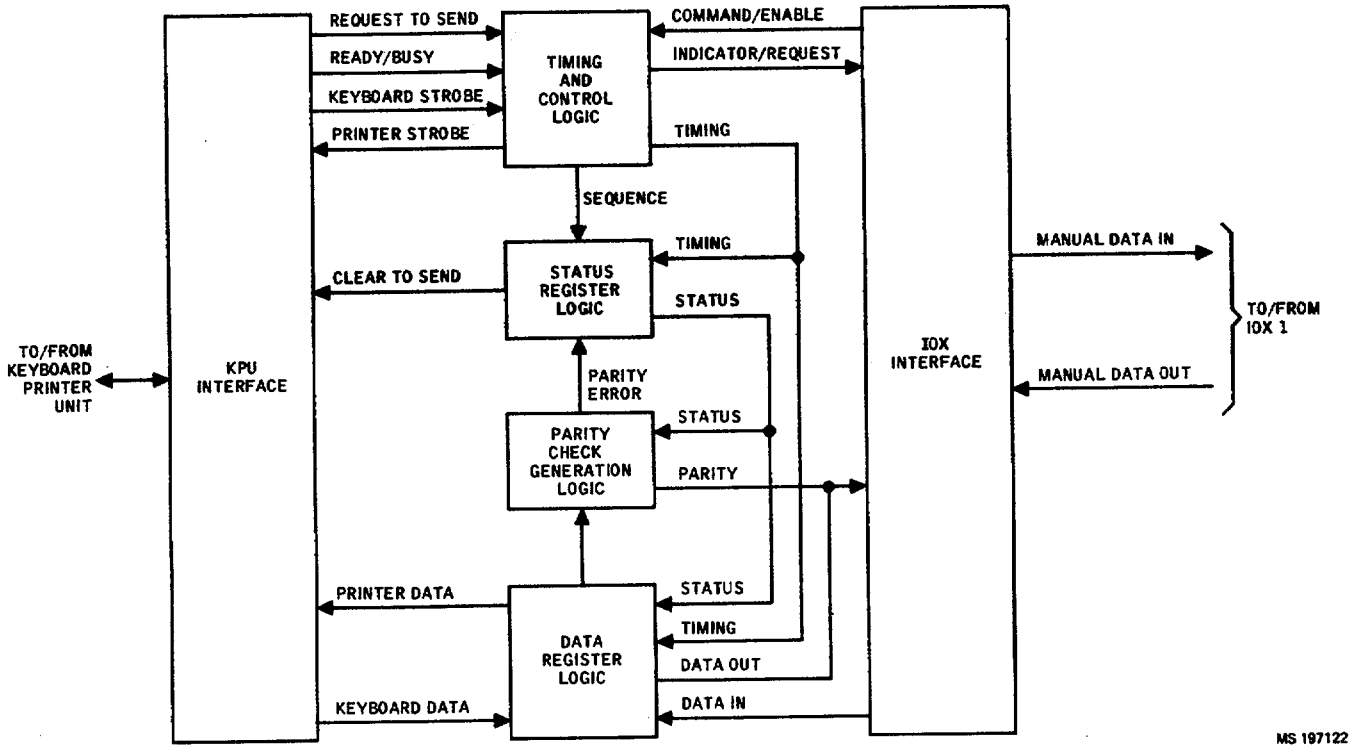

Figure 2-24. Keyboard Printer Unit Controller Block Diagram

a. KPU Program Control Responses. The KPU responds to computer-generated commands as specified in the following subparagraphs.

(1) DEV operation. The DEV command consists of an address selection phase using the command line, a control phase with information lines 0 and 3 activated, followed by a single byte of information that is used by the KPU controller for control purposes. The KPU controller acknowledges receipt of this command sequence by activating the indicator line after receiving the data byte. Upon receipt of the command byte, the controller performs the following:

Command byte	Response
0000 1100	Enter automatic input
0000 1001	Enter automatic output
0000 1010	Device halt enter standby

(2) OFR operation The OFR command has an address selection phase using the command line, a device control phase with information lines 0 and 4 activated followed by four data bytes. The OFR operation places the controller in the test mode. The controller acknowledges receipt of the device control byte by activating the indicator line.

(3) ITR operation. The ITR sequence has an address selection phase using the command line, a device control phase using information lines 0 and 5, followed by one data byte generated by the controller. The KPU controller activates the indicator line when sending the data byte. The status byte format is shown in table 2-16.

(4) EOB operation. The EOB sequence has an address selection phase using the command line followed by a controller control phase using information lines 0 and 6. When the controller detects EOB, the controller returns to the idle state and initiates an interrupt sequence.

(5) Device stop operation. The stop sequence has an address selection phase using the command line followed by a control phase using information lines 0 and 7. The sequence is generated by the KPU computer when an illegal or erroneous condition occurs as related to the controller. When the controller detects this operation, the controller reverts to the standby state.

(6) Master reset operation. The master reset operation occurs when the command line and enable line are active simultaneously. The address (information) lines are ignored during a master reset operation. When the KPU controller detects this operation, the controller reverts to the standby state.

(7) Command priority. The last given command is obeyed. All other controls are reset, except if the command is an ITR command, the controller is not reset.

Table 2-16. Keyboard Printer Unit Status Byte

Bit no.	Significance	Explanation
0 (MSB)	Spare	
1	Spare	
2	Input mode	Controller is in the input mode
3	Output mode	Controller is in output mode
4	Test mode	Controller is in test mode
5	EOB	EOB recurred during input mode
6	Overflow	At least one byte has been output with a parity error
7 (LSB)	Parity error	Computer did not accept input data byte before next byte was input from keyboard

MSB - Most significant bit.
LSB - Least significant bit.

b. KPU Controller Mode Responses. The KPU functions to be performed for each mode of the controller are as specified in the following subparagraphs.

(1) Operator-initiated input mode. For the operator-initiated input mode, the program establishes the controller channel keyword with a maximum block length and with the input-by-byte mode specified. The program also establishes the termination word to the external interrupt condition. The program then places the controller in the input mode with a DEV sequence. Subsequent to the address and control phases, the program outputs byte 00001100 to the controller. Receipt of the byte during a DEV operation causes the controller to enter the data input state. While in this state (except when the input data register contains an input character that has not yet been delivered to the computer), the controller activates the clear-to-send signal to the keyboard. The presence of this signal causes the corresponding indicator on the keyboard to light. While the indicator is lighted, the operator can use the keyboard to input data to the computer. Pressing a key causes the keyboard electronics to input a character over the data lines in the six-bit ASCII code. Within a minimum of 150 microseconds after the data lines have been activated, the keyboard generates a strobe signal. The strobe signal causes the controller to accept the character present on the data lines. The controller simultaneously outputs the character to the printer, and requests input to the program by activating the request sequence. When the operator completes a message, he generates an EOM signal by pressing the REQUEST TO SEND switch on the KPU keyboard. Receipt of this signal causes the controller to perform an external interrupt sequence. A status byte is input with the external interrupt sequence. If the input message exceeds the block length in the keyword, the computer initiates an EOB sequence. If this occurs, the controller sets the overflow bit in the status byte. In response to the EOB signal, the controller inputs the status byte, including the overflow bit. This alerts the program to reestablish the input buffer area and the keyword and termination word input conditions. Following the external interrupt sequence, the controller enters the standby mode and remains in this mode until otherwise commanded by the program.

(2) Output mode. In the output mode, the KPU can print only program-initiated data. To enter this mode, the program establishes the output message in a buffer area in the memory. A channel keyword is then established with its current address referenced to the buffer area, appropriate block length, and designated byte output mode. The termination word is set. to allow for external interrupt. A DEV sequence is initiated to place the KPU controller in the output mode. This DEV uses the control byte 00001111. On detection of this byte in a DEV sequence, the controller enters the output mode. By use of the request sequence, the controller obtains data bytes from the computer. The rate of output is determined by the ready/busy signal activated by the printer. At the end of the message, the computer issues an EOB sequence. On receipt of the EOB sequence, the controller transmits an external interrupt signal accompanied by a status byte (see table 2-16). If an error condition exists, the controller does not halt operation but sets the appropriate status bit and prints the circumflex 2< :W> in place of the character to be printed, indicating a parity error. The controller then resumes the standby mode.

c. KPU Test Mode Responses. The program causes the KPU to operate in the test mode by initiating an OFR sequence. The first OFR data byte is an eight bit character or test message. The other three bytes in the message are ignored. The program defines a keyword and termination word appropriate to the test sequence. On receipt of the test message in the OFR sequence, the KPU controller enters the input mode and request input service. Return of the message plus parity without error is considered a successful test. On completion of the test, the computer initiates an EOB sequence. The controller responds with an external interrupt accompanied by the status byte. The controller then assumes the standby mode.

d. KPU Standby Mode. The KPU returns to the standby mode as a result of any of the following: an EOB sequence, a device stop, an EOM switch input from the keyboard in the input data state, a master reset, or a software DEV halt. The KPU controller remains in the standby mode until receipt of its command. The controller then responds as described in para 2-12a(2).

e. KPU Code Conversion. The KPU controller converts the 7-bit ASCII code transmitted from the computer to a 6-bit ASCII code compatible with the keyboard. The controller receives the 6-bit ASCII code from the keyboard and coverts the code to the 7-bit ASCII code compatible with the computer.

f. KPU Typewriter Operation. The KPU can be used only as a typewriter with no computer input of typed data on the printed page when the ON LINE/ OFF LINE switch is placed in the OFF LINE position.

2-13. Magnetic Tape Unit (MTU) Overall Operation. Two identical MTUs are used in the AN/TSQ-73 system. The MTUs provide peripheral data storage and software program input capabilities. The MTUs interface with the IOU, using addresses 10 and 11. During on-line operation, the MTUs are under complete control of the ADP. However, they can be operated off-line for read/test functions and tape wind/rewind operations.

The MTU operations can be grouped into read, write/ erase, and position functions. A block diagram of the MTU is shown in figure 2-25.

a. Read (to IOX). The ADP establishes a keyword and termination word corresponding to the MTU address and operation to be performed (program load). The IOU, on receipt of a device command from the computer generates a device command byte which is transferred to the I/O timing and control logic of the MTU. The I/O timing and control logic transfers the device command to the command and timing control logic. This command byte specifies the operation to be performed, such as read, space forward, space reverse, high-speed forward, or reverse. A start signal is generated and applied to the motor control logic of the cartridge interface logic. When the tape transport is at the proper speed, a read strobe signal is generated and the read data from the tape is stroked into the data handling logic. A request signal is generated by the command and timing control logic and transferred to the IOX. The ADP then transmits an enable signal to the I/O timing and control logic. The enable strobe is applied to the data handling logic and the register (tape) data is transferred to the I/O timing and control logic. The I/O timing and control logic converts the data bytes to levels usable by the ADP, and transfers them to the IOX. When the last byte is transferred, an interrupt sequence is initiated. If the ADP does not return another forward or read command, the tape is stopped by the command and timing control logic and the MTU returns to the standby condition.

b. Write Erase (from IOX). The write/erase process is initiated in the same manner as the read operation. However, the command word contains the write/ erase command. Once the command and timing control logic senses that the motor is up to speed, the write data is stroked into the cartridge interface logic and recorded on the tape. When all the data is transferred, and the last EOB received an interrupt sequence is initiated to the IOX. If no additional write/erase commands are received, the tape is halted and the MTU reverts to the standby condition. During data transfer (to the data handling logic), the data bytes are checked for parity errors. If an error exists, a status bit is set in the data handling logic and an interrupt sequence is initiated. For the MTU to perform the write process, the write-enabled line from the control panel interface logic must be active. For the write-enabled line to be active, the tape cartridge write protect cam must be off the PROT position, the MTS test shorting connector must be in place, the MTU must be on-line, and the front panel WRITE ENABLED switch lighted.

2-14. Magnetic Tape Unit (MTU) Detailed Description.

a. Basic Operation of MTU. The basic actions performed by the MTU are read, write, and position operations. To initiate any of these operations, the computer transmits a device command to the MTU (or any

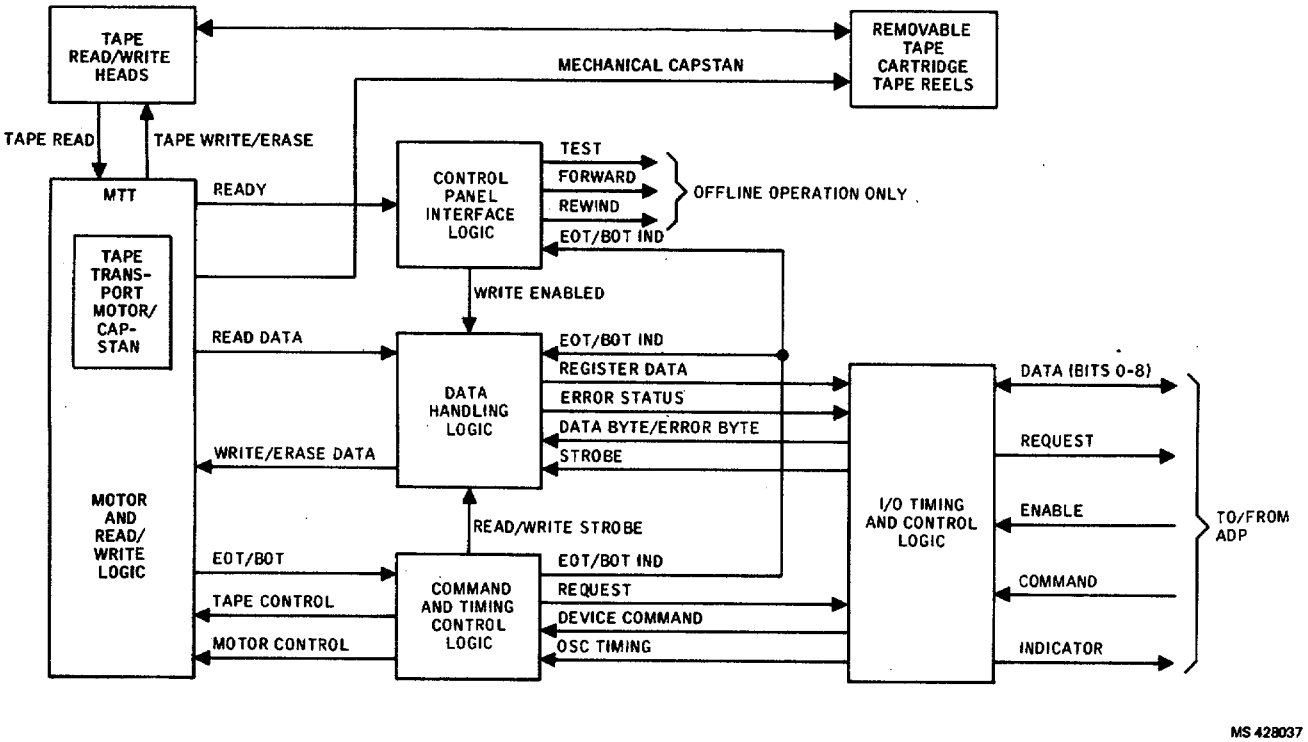

Figure 2-25. Magnetic Tape Unit Block Diagram

other peripheral unit). The MTU acknowledges the device command by pulsing its indicator line. In addition to the signal on the indicator line, the MTU generates internal instructions to the tape transport motor to move the tape at the prescribed speed, either normal (25 inches-per-second) or high (50 inches-per-second). Normal speed is used for read-and-write operations, and high speed is used for moving rapidly to a more distant portion of the tape (approximately 450 feet in length).

b. Construction Features. The MTU contains two major subassemblies designated the MTU electronics and the Magnetic Tape Transport (MTT) assembly, which contains a removable Magnetic Tape Cartridge (MTC).

(1) MTU electronics. The MTU electronics contains all digital and analog circuit cards used to process data. The cards are mounted in a standard card rack assembly. All control and command logic needed to perform the required functions is contained on 64 printed circuit cards. Logic elements including gates, flip-flops, and inverters, are mounted on circuit cards which are interchangeable with any other card of the same type in the system. For example, any flip-flop card with a given part number can be exchanged with any other flip-flop card bearing the same part number.

(2) Magnetic tape transport (MTT) assembly. The MTT contains the electronic and mechanical components required to control and move tape in the tape cartridge. The tape cartridge is a self-contained unit enclosed in a plastic case. It is inserted into the MTU through a door on the MTU front control panel. The cartridge contains a 450-foot magnetic tape and two reels on which the tape is wound. When the cartridge is inserted, a boss in the MTT pushes open a door on the front edge of the tape cartridge to allow the tape to press up against the read/write head and the tape motor capstan in the MTT. Thus tape can be moved and either read from or written on, depending on ADP or manual commands to the MTT.

(a) MTT description. The MTT contains the tape read/write heads, a motor/tachometer motor drive assembly, and circuit cards to control tape movement and read/write functions. The tape read/write heads consist of nine read and nine write channels and provide a read/write density of 800 bits-per-inch per channel. The write current is approximately 25 ma. The motor/tachometer is a two-speed bidirectional dc motor concentric with the tachometer. The motor capstan moves tape in either direction at 25 ips (read/write) and 50 ips (fast forward/reverse). The tachometer enables the MTT to maintain a constant tape speed during operation. Optical sensors in the MTT sense the beginning-of-tape (BOT) and end-of-tape (EOT). BOT and EOT sensors feed into tape control circuits to prevent tape from overrunning on the reels, or the heads from writing on the tape leaders.

(b) Tape cartridge. The removable tape cartridge contains the magnetic tape wound on two reels, each reel approximately 2.4 inches in diameter. An internal drive belt and tensioning devices hold the tape in constant tension regardless of the amount of tape on either the supply reel or the takeup reel. The tape is mylar-base, 0.5 inch wide, and 1.2 mils thick.

c. Peripheral Unit Data Format. Information is stored on the tape in the form of bytes. A byte consists of eight information bits and a parity bit. Each bit is recorded in channels across the tape by one of nine write-head channels. Associated with each channel is a write-head channel and a read-head channel. A single group of bytes on the tape can vary from 2 to 32, 768 bytes, which constitute a record. Before and after each record there is an interrecord gap of approx 3-H57; to 3-H42; inches of tape. A special byte, called the Longitudinal Redundancy Check (LRC), is written immediately (three byte spaces) after the last data byte of a record. This byte is used in checking the accuracy of the data being processed. Internally, the computer operates in 32-bit words and 8-bit bytes. Words and bytes are composed in blocks and the computer records information in blocks. Communication with any peripheral device is controlled by keywords. A keyword contains information on the number of words or bytes to be involved in any device operation. As the data transfer takes place, the computer decrements the block portion (or field) of the keyword. When the block field is decremented to zero, the computer issues an EOB command to the peripheral device. In the MTU, an EOB counter is used. The MTU can transfer up to 16 blocks (2048 bytes) of data before terminating the command. In an operation such as read, the EOB counter in the MTU is preset to the desired number of blocks. As the block field portion of the keyword is decremented, the EOB commands cause the EOB counter in the MTU to be decremented. The operation is ended when an EOB command occurs at the same time that the EOB counter is at zero. If a read operation is being performed, no more data is transmitted to the computer. However, since the MTU tape can be within a record, the tape is kept moving until the next interrecord gap is reached before a tape stop sequence is performed. As the tape enters the interrecord gap, a look-ahead operation is performed, and the tape is either stopped or kept moving as determined by additional commands from the computer.

d. MTU Operating Modes. The MTU operation includes on-line and off-line operations. Off-line operations comprise only turn-on and self-test operations. On-line operations are completely automatic under the control of the system computer. Although the MTU operates primarily in either a read or write mode, several other operations are provided under the control of commands received from the computer, and are described in the following paragraphs.

e. MTU Operation in Response to Device Command. A description of device commands, and the operations performed by the MTU in response to them, are as follows:

(1) Write. The device command sequence, which initiates a write operation, is accomplished in the initial address selection phase, during which a specific command is followed by a byte containing specific control information. The indicator line is used to acknowledge receipt of the command only and not to indicate that the MTU is ready to receive data. The IOU will then supply data bytes to be written on the tape in response to requests from the MTU in the automatic output mode. During the command phase, a block counter in the MTU is preset to the desired count. When the last data byte of the last block is received, the block counter indicates a zero count and the write-terminate phase is entered when the last EOB is received. The write terminate phase consists of encoding and writing the LRC character, generating the Inter-Record Gap (IRG), and initiating an interrupt sequence. If another write or erase command is not received within five milliseconds, the stop sequence is initiated. Since the number and length of records on a given tape are both variable, a method of locating a specific record is needed. For positive identification, the first two or more bytes of each record can contain a record identifier.

(2) Read. The device command sequence which initiates a read operation is accomplished in the initial address selection phase, a device command byte, followed by a byte containing specific control information. At the end of these three phases, the MTU signals that it is ready to read by activating the indicator line. The MTU then reads each byte of the record and follows each with a request on the request line. As with the write operation, the block counter keeps track of the read operation, and when the counter has been decremented to zero and an EOB command is received, the data transfer is terminated. All operations are terminated by an interrupt sequence. The interrupt sequence serves two purposes: (1) to signal the end of the operation and (2) to indicate the accuracy of transmission. The accuracy can be compromised by the following types of errors: tape parity, no-data, BOT, EOT, computer data parity error, timing, motor error, and file protect error. An interrupt can be sent by the MTU for any of these types of errors.

(3) Space forward. The space forward device command is used to advance the tape to a given area of the tape to prepare to read or write a specific location. During a space forward device command, the MTU moves the tape forward at normal speed and detects interrecord gaps. The block counter is used to count the desired number of interrecord gaps before the interrupt sequence is generated. This allows the MTU to move the tape forward a distance equivalent to 16 records while generating only one interrupt sequence. The tape stops with the head positioned in the interrecord gap.

(4) Space reverse. The space reverse device command is identical to the space forward device command except for the direction of tape movement.

(5) Erase forward. The erase forward device command sequence commands the tape to move forward at normal speed and causes a fixed length of tape (approx 2 inches) to be erased. An interrupt sequence is generated upon completion of the 2-inch erase operation. As with the previous commands, if an additional erase command is received within 5 milliseconds, the tape will keep moving. Otherwise, a stop sequence is initiated.

(6) Erase reverse. During the erase reverse command, the data recorded is erased until an interrecord gap is detected. If another command (requiring the same tape speed and direction) is received within 5 milliseconds, the tape will continue to move. Otherwise, a stop sequence is performed. This command makes it possible to remove a data record without affecting the records on either side.

(7) High speed forward. The high speed forward device command initiates a sequence in which the tape is moved forward at high speed. While the tape is in motion, interrecord gaps are detected and a request signal is generated. These requests are counted by the computer in the alarm mode. The computer can cause the tape movement to be stopped by generating an EOB command.

(8) High speed reverse. The high speed reverse device command is identical to the high speed forward command except for the direction of tape movement. When the tape movement in either high speed forward or reverse is stopped by an EOB command from the computer, the tape cannot stop within an interrecord gap. Consequently, a space forward operation must be initiated to position the read/write head in the next interrecord gap. A read operation must then be initiated to read the record identifier bytes to determine the exact position of the tape. Each of the two high speed commands is followed by an. interrupt generated by the MTU.

(9) Rewind-to load point. During the rewind-to-load point device command, the tape is rewound at high speed to the beginning of the tape. The command is completed when the BOT sensor is actuated and a stop sequence is generated. An interrupt signal is generated by the MTU at the completion of the command.

2-15. DC/DC Converters. Each dc/dc converter converts shelter + 135v to lower voltages to power the ADP equipment logic circuits. An internal fault monitor circuit lights an indicator on the converter if a fault occurs. External voltage faults cause a second indicator on the converter to light.

2-16. Memory Power Supplies. Each 32K MU is powered by a power supply that converts shelter + 135 vdc to the voltages required by the MU logic circuits. A fault monitor circuit lights an indicator on the power supply if an internal fault occurs. The power supply generates the following voltages: +5 vdc at 10A, -5 vdc at 0.5A, and +12 vdc at 0.75A. The power supply also generates an auxiliary +5 vdc used to power the POWER ON and POWER FAULT indicators on the control panel. The power supplies are integral with the MUs.

2-17. ADP Status and Control Panel. This panel includes all of the controls required to operate the ADP equipment, and also houses all ADP equipment indicators except those on the dc/dc converters and memory power supplies. Four Light-Emitting-Diode (LED) numerical displays are provided to aid in fault isolation.

CHAPTER 3

COMPONENT LOCATION AND FAULT ISOLATION/TROUBLESHOOTING

Section I. GENERAL

3-1. Scope. This chapter provides the maintenance information required to permit field personnel to troubleshoot the ADP equipment to a replaceable circuit card, module, or rack-mounted component. Maintenance data provided includes component location illustrations, fault isolation flow charts, removal and replacement procedures, cabling and wiring diagrams, and tools and test equipment. Reference to preventive maintenance and alinement procedures are included to facilitate routine maintenance and inspection of the equipment.

3-2. Emergency Power Shutdown. For emergency power shutdown of system power, press SYSTEM POWER OFF switch on power cabinet power transfer unit. Observe that SYSTEM POWER ON indicator goes out.

3-3. Normal Shutdown Procedure. For normal shut- down procedures, refer to Operator's Manual TM 9- 1430-652-10-3.

3-4. Tools and Test Equipment. Tools common to electronics equipment maintenance are stored in the issue box or storage drawers in the maintenance bench. Test equipment is stored in the maintenance bench and storage area. These tools and test equipment are listed in Overall System Maintenance Manual TM 9-1430- 655-20-1.

3-5. Preventive Maintenance Procedures. Preventive maintenance is the systematic care, inspection, and service of the ADP equipment to provide maximum operational capability. Preventive maintenance procedures are contained in Overall System Maintenance Manual TM 9-1430-655-20-1.

3-6. Alinements and Adjustments. No alinements or adjustments to the ADP equipment are necessary.

Section II. COMPONENT LOCATION

3-7. General. This section explains the reference designator system for the ADP, and illustrates the location of components applicable to on-site maintenance.

3-8. Reference Designators. Each subassembly, control panel, and circuit card used in the ADP is identified by a reference designator. The reference designator system used follows a descending order, starting with the shelter as the top assembly, followed by major equipment, major subassembly, unit, card bay, card shelf, and card slot. As an example, reference designator 1A1A3A31103 is interpreted as follows:

1	A1	A3	A6	A1	1	03
Shelter	Equip-ment Rack	Rack 3	32K Memory	Bay	Card Shelf	Card Slot

Table 3-1 lists the ADP equipment, exclusive of bay, shelf, and card slot, in reference designator order.

Table 3-1. Automatic Data Processor, Reference Designators

Reference designator				
Unit	Major equipment	Major subassembly	Subassembly	Component
1				Shelter
	A1			Equipment rack
		A2		Rack 2
			A1	ADP status and control panel
			A3	Spare (memory growth)
			A4	Spare (memory growth)
			A8	Spare (memory growth)
			A9	Spare (memory growth)
1	A1		A3	Rack 3
			A1	IOU
			A2	Buffer unit
			A3	Upper CPU (bay 1 and 2)
			A4	Lower CPU (bay 1 and 2)
			A5	32K memory unit (4-port)
			A5PS1	Dc/dc converter
			A6	32K memory unit (4-port)
			A6PS1	Dc/dc converter
			A7	32K memory unit (4-port)
			A7PS1	Dc/dc converter
			A8	32K memory unit (4-port)
			A8PS1	Dc/dc converter
			PS1 through PS6	Power supplies
		A6		ADP interface panel

3-9. Circuit Card Description. Both digital and analog circuit cards are used in the ADP, as shown in figures 3- 1 and 3-2. Two different sizes of digital circuit cards are used, one of which is 1-1/4 by 5-1/2 inches and the other is 4-1/8 by 5-1/2 inches. All analog circuit cards are 4-1/8 by 5-1/2 inches. Both analog and digital circuit cards have 80-pin etched connectors. The connector pins are grouped in two rows of 40 pins with one row on each side of the circuit card. The odd numbered pins are located on the component side of the circuit card. The even numbered pins are located on the back side. Each different type of circuit card is keyed by slots cut in the connector. Corresponding keys in the card cage circuit card connectors prevent the insertion of any circuit card except the properly keyed card. Test points are etched on the side opposite from the connector pins. The digital circuit cards have either 40 or 80 test points, and the analog circuit cards have 24. With the circuit cards installed, the test points are accessible using special test point connector adapters.

3-10. Circuit Card Color Coding. Circuit cards used in the ADP are color coded by part number. Two basic series of part numbers are used for circuit cards, the 1028XXXX series and the 5871XX-XXX series. Color code zones for each of the two circuit card part number series are shown in figure 3-3. The color codes conform to the standard resistor color code. With the 1028XXXX series circuit cards, the last four digits of the part number are represented by colors painted in zones 1 through 4 on the circuit card edge. With the 5871XX-XXX series circuit cards, some circuit cards are not color coded and some circuit cards are color coded with only one or two colors. When used, a color in zone 1 represents the tens digit of the basic part number. A color in zone 3 represents the units digit. In both series of circuit cards, corresponding colors are painted on the card edge circuit card retainers.

3-11. ADP Component Location. All of the ADP equipment is located in electronics racks 2 and 3 (1A1A2 and 1A1A3).

a. *Rack 2 Equipment* Figure 3-4 shows ADP equipment locations in rack 2. Power cables required for memory expansion are connected to brackets installed in door A. Figure 3-5 shows locations of components on the ADP status and control panel. Figure 3-6 is a schematic diagram of component assemblies A4 and A5.

b. *Rack 3 Equipment*. Figure 3-7 shows ADP equipment locations in rack 3. Table 3-2 lists ADP power supplies and the units they power. Figure 3-8 shows component locations in the 32K memory units. Table 3-3 gives card locations in the 32K memory units. Figure 3-9 shows component locations in the IOU. Table 3-4 gives IOU card locations. Figure 3-10 shows component locations in the buffer unit. Table 3-5 gives card locations of the buffer unit. Figure 3-11 shows the component locations in the two identical CPUs. Table 3-6 gives CPU card locations.

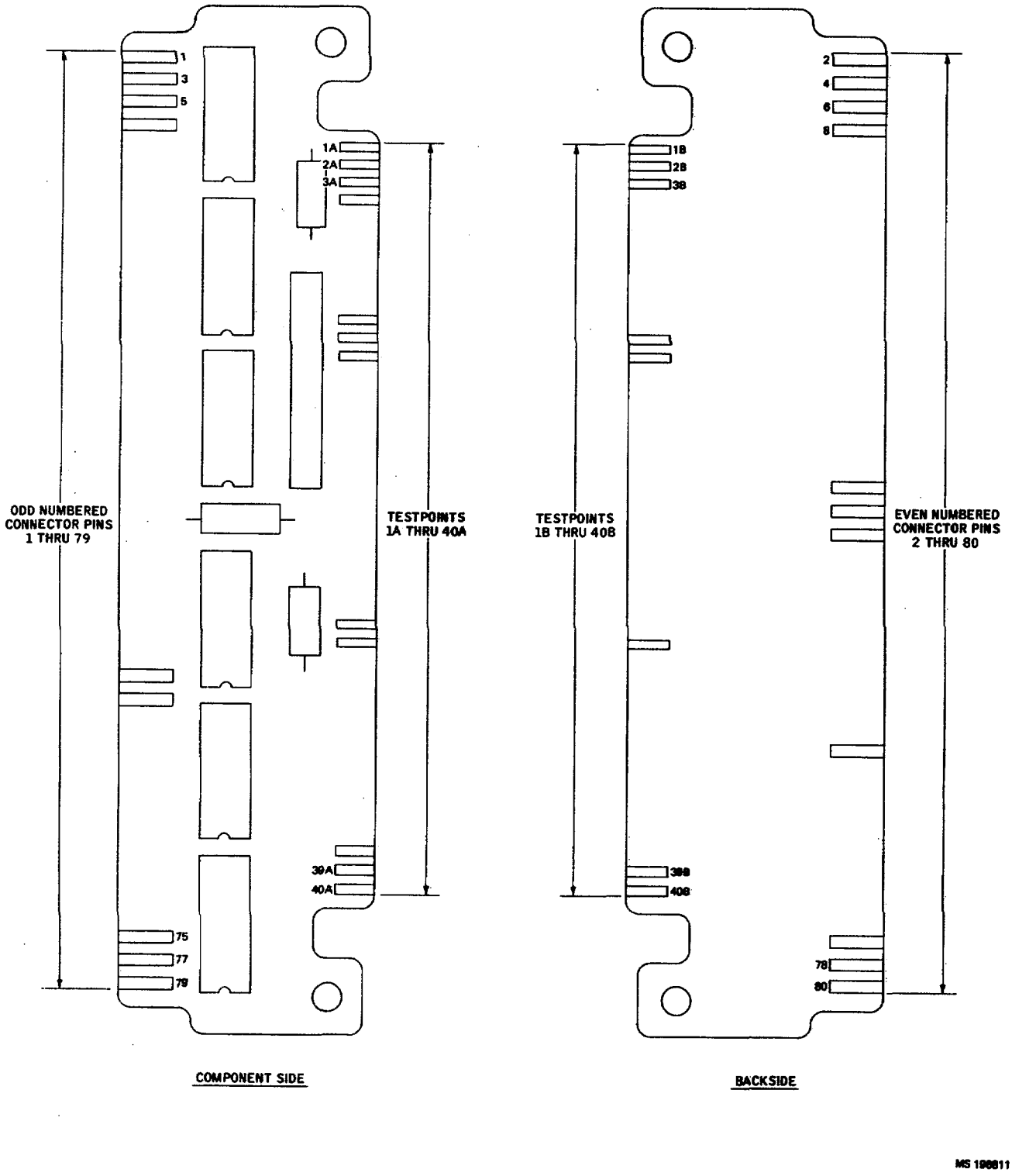

Figure 3-1. Typical Digital Circuit Card

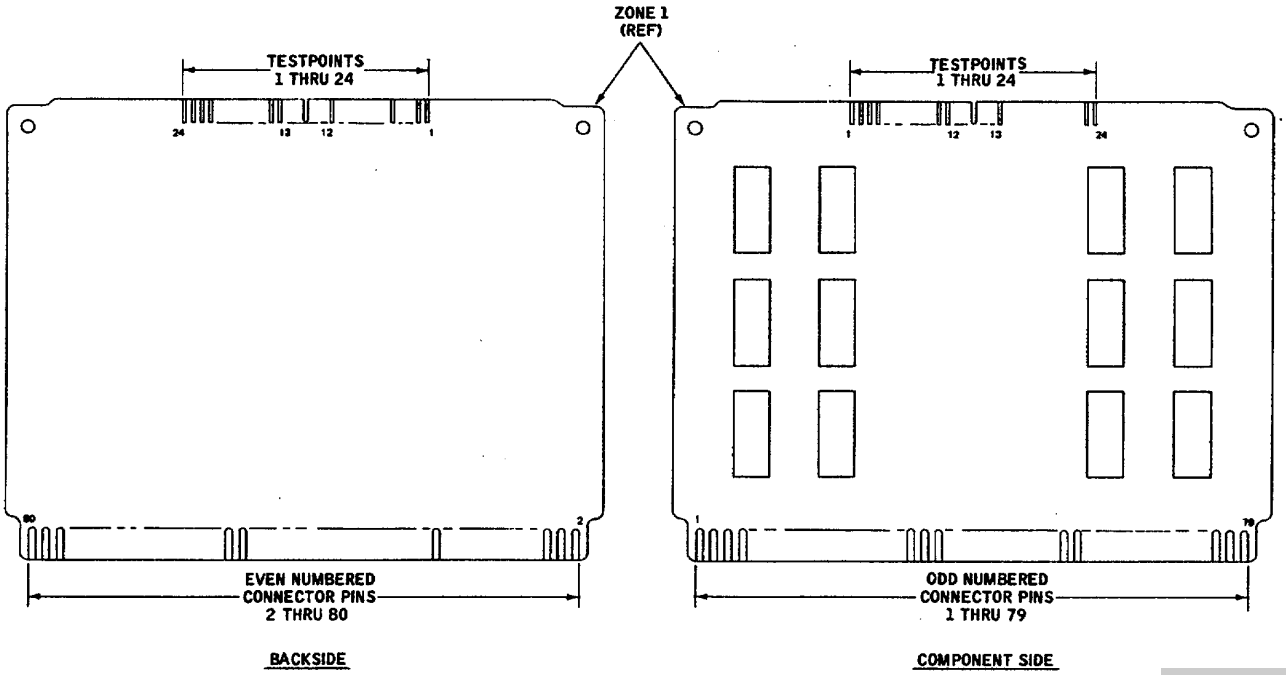

Figure 3-2. Typical Analog Circuit Card

NOTES:

1. COLOR CODES ARE USED ON CIRCUIT CARDS AND CARD CAGE CARD SLOTS. CIRCUIT CARDS ARE MARKED ON EDGE TABS AND CARD SLOTS ARE MARKED WITH COLOR DOTS ON CARD GUIDES.
2. ON 5871XX-XXX SERIES CIRCUIT CARDS, ONLY ONE- OR TWO-COLOR COLOR CODES ARE USED; ON 1028XXXX SERIES CIRCUIT CARDS, A FOUR-COLOR COLOR CODE CORRESPONDING TO THE LAST FOUR DIGITS OF THE CIRCUIT CARD PART NO. IS USED.
3. REFER TO CARD COMPLEMENT TABLES FOR APPLICABLE CIRCUIT CARD COLOR CODES.

COLOR CODE	
COLOR	VALUE
BLACK	0
BROWN	1
RED	2
ORANGE	3
YELLOW	4
GREEN	5
BLUE	6
VIOLET	7
GRAY	8
WHITE	9

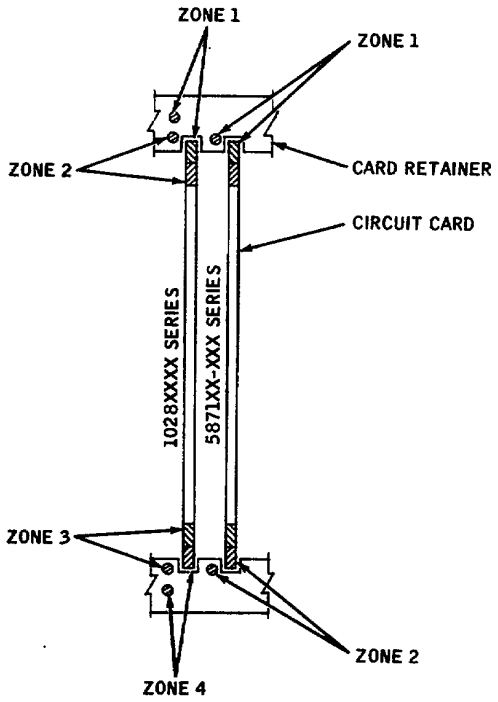

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Figure 3-3. Circuit Card Color Codes

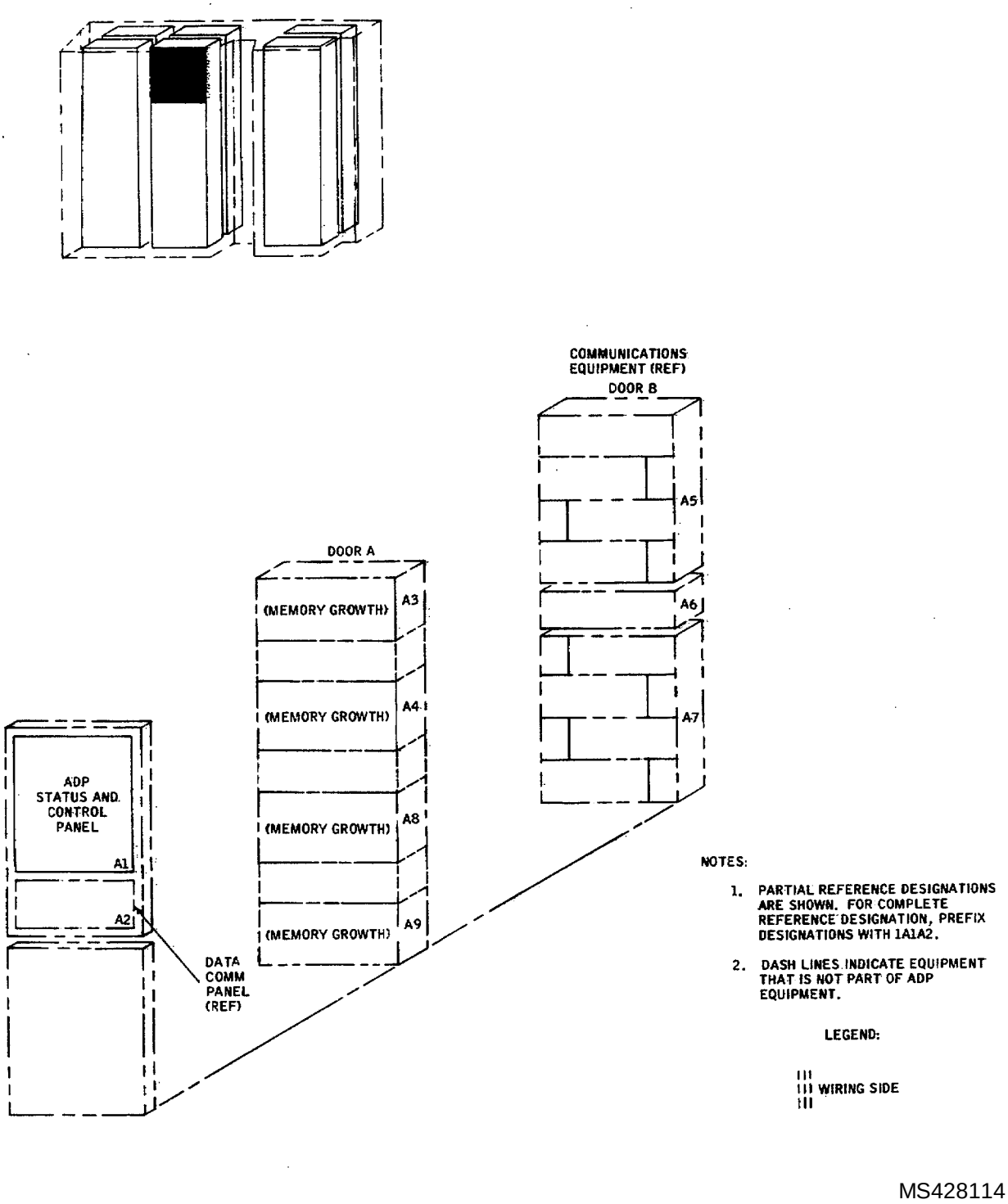

Figure 3-4. Automatic Data Processor Rack 2, Equipment Locations

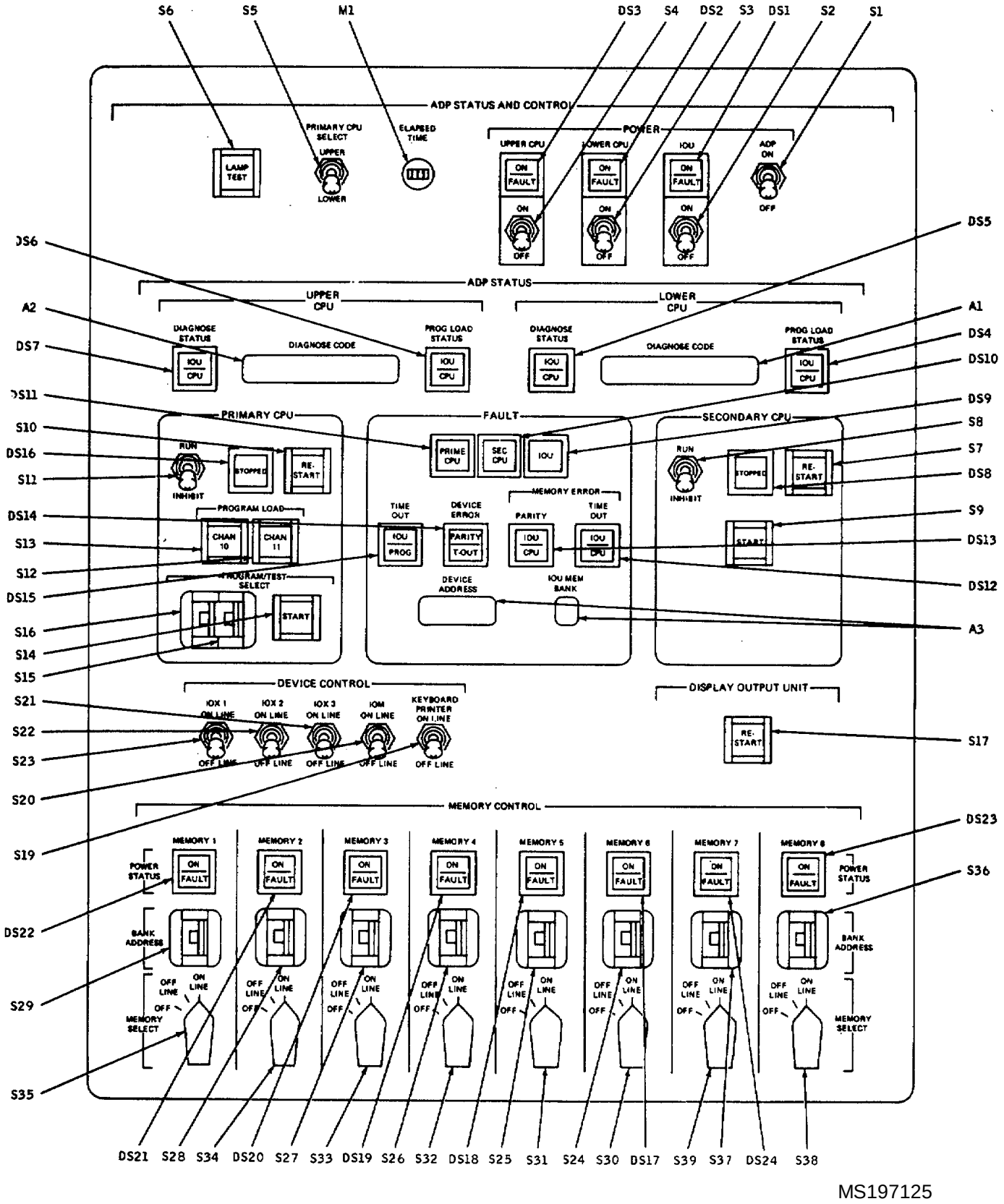

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Figure 3-5. Automatic Data Processor Status and Control Panel 1A1A2A1, Component Locations (Sheet 1 of 2)

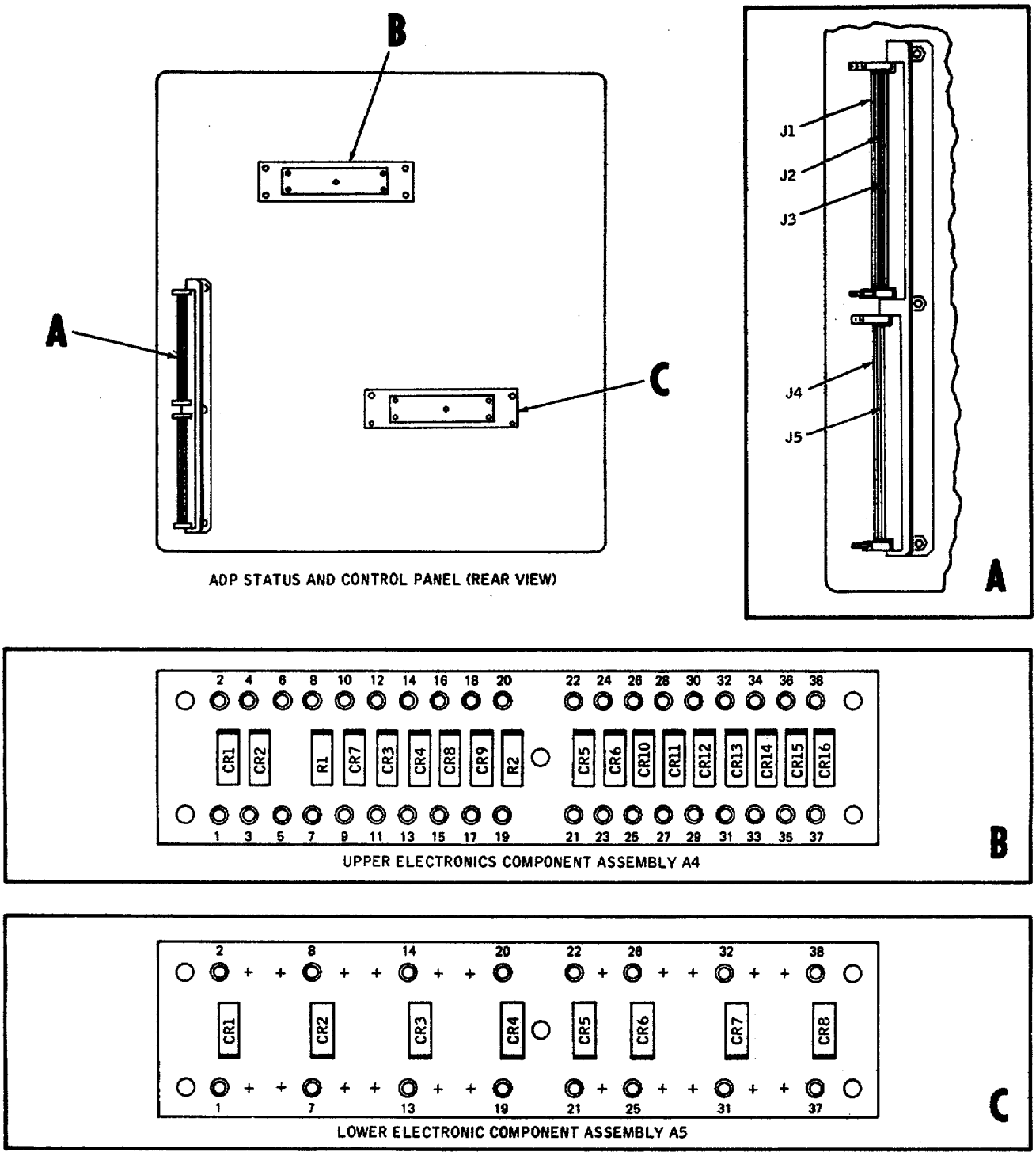

Figure 3-5. Automatic Data Processor Status and Control Panel 1A1A2A1, Component Locations (Sheet 2 of 2)

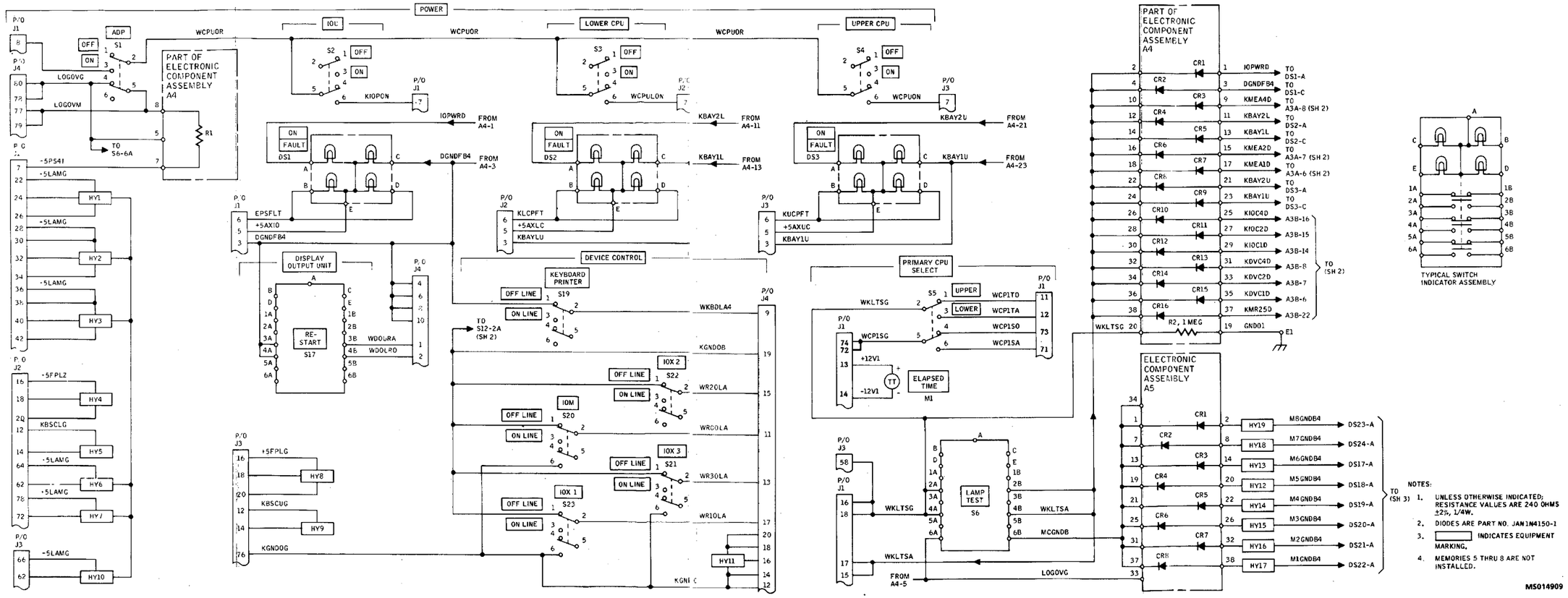

Figure 3-6. Component Assemblies A4 and A5 Schematic Diagram (Sheet 1 of 3)

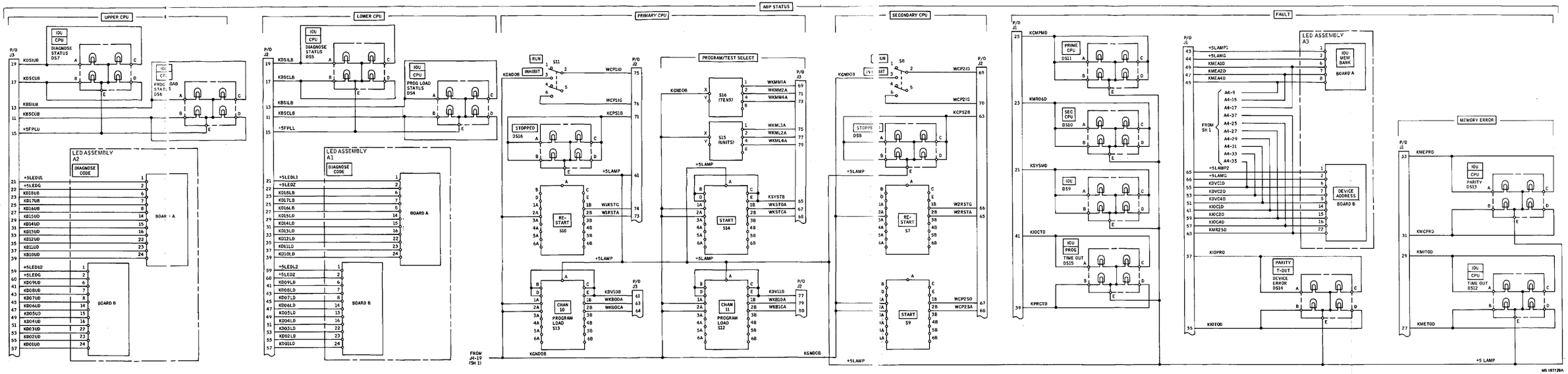

Figure 3-6. Component Assemblies A4 and A5 Schematic Diagram (Sheet 2 of 3)

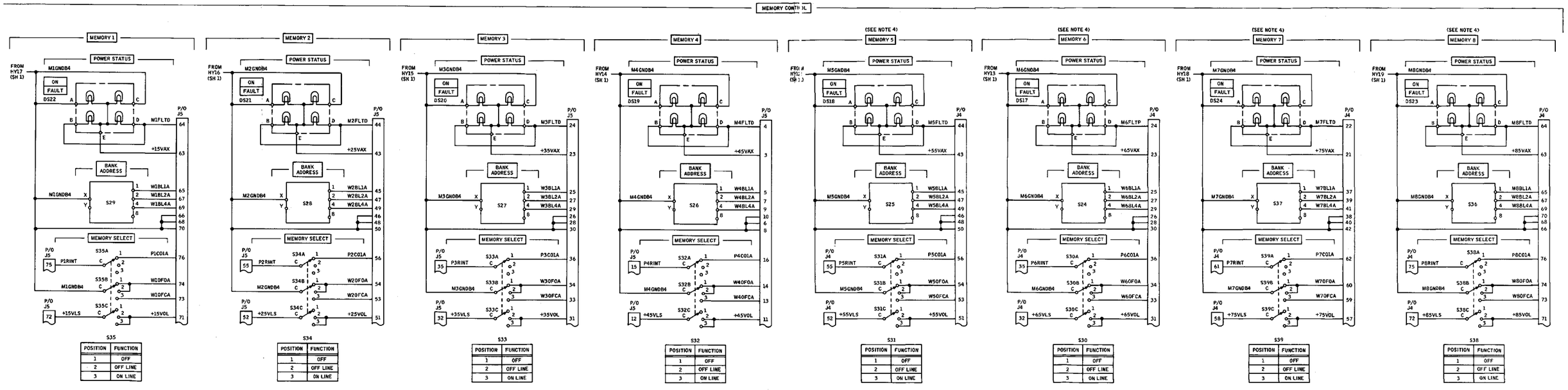

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Figure 3-6. Component Assemblies A4 and A5 Schematic Diagram (Sheet 3 of 3)

CHART 1

BUFFER UNIT FUNCTIONAL CARD LOCATION	
FUNCTION	CARD LOCATION
KPU CONTROL	A1112 THRU A1148
DISPLAY OUTPUT UNIT	A1201 THRU A1246, A1301 THRU A1311
IOX2	A1327 THRU A1345
IOX1	A1427 THRU A1445
IOE1	A1313 THRU A1318
IOE2	A1320 THRU A1325
IOE3	A1406 THRU A1411
IOE4	A1413 THRU A1418
IOE5	A1420 THRU A1425

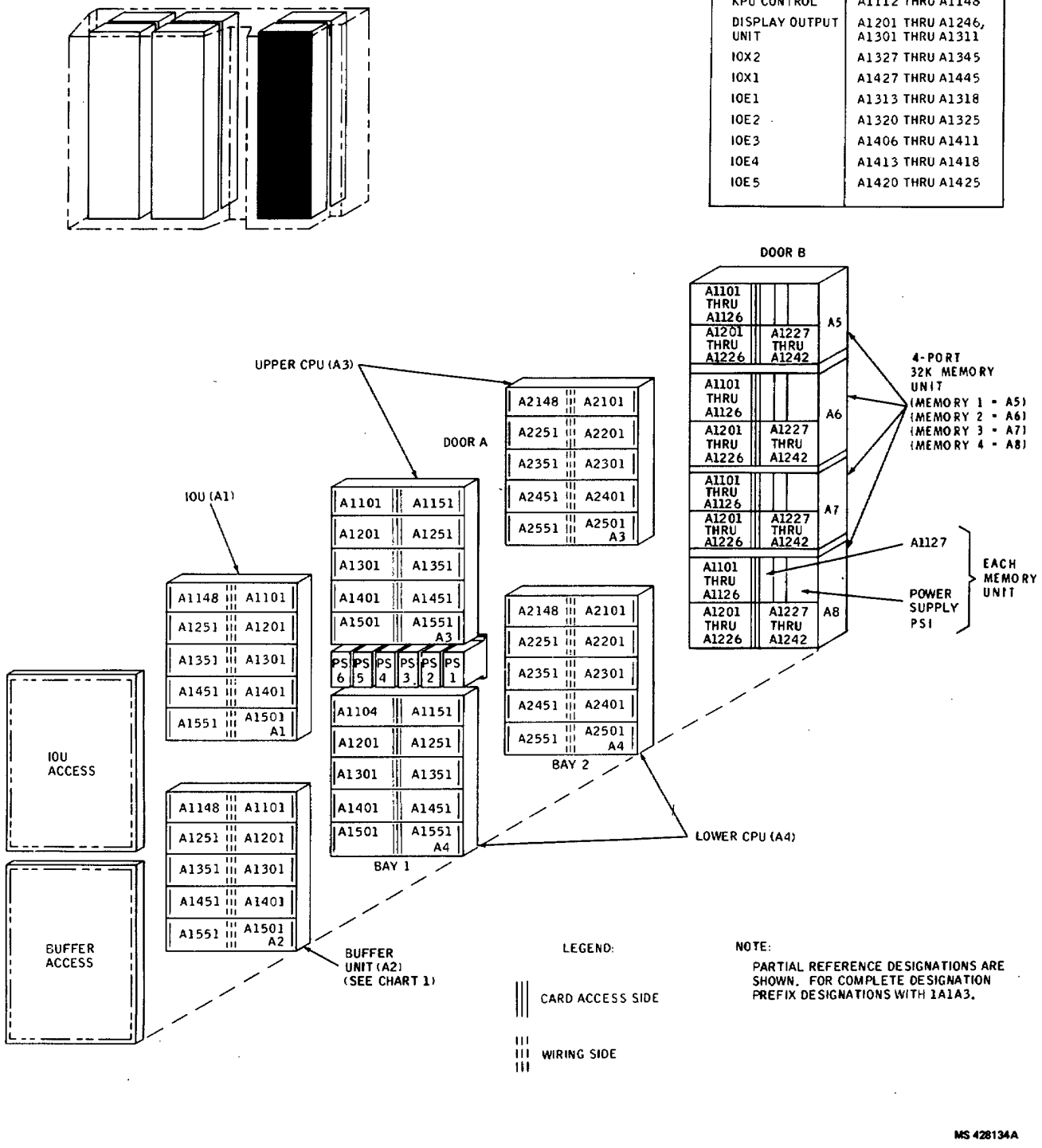

Figure 3-7. Automatic Data Processor Rack 3, Card Locations

Table 3-2. Automatic Data Processor Power Supplies

Power supply	Part number*	Power supply type	Units powered
Rack 3-1A1A3			
PS1	126649-102	DC/DC converter	CPU, lower bay 1
PS2	126649-102	DC/DC converter	CPU, lower bay 2
PS3	126649-102	DC/DC converter	Buffer unit
PS4	126649-102	DC/DC converter	IOU
PS5	126649-102	DC/DC converter	CPU, upper bay 1
PS6	126649-102	DC/DC converter	CPU, upper bay 2
A5PS1	126649-102	DC/DC converter	32K memory unit, 4-port (A5)
A6PS1	126649-102	DC/DC converter	32K memory unit, 4-port (A6)
A7PS1	126649-102	DC/DC converter	32K memory unit, 4-port (A7)
A8PS1	126649-102	DC/DC converter	32K memory unit, 4-port (A8)

*126649-101 is acceptable alternate for 126649-102.

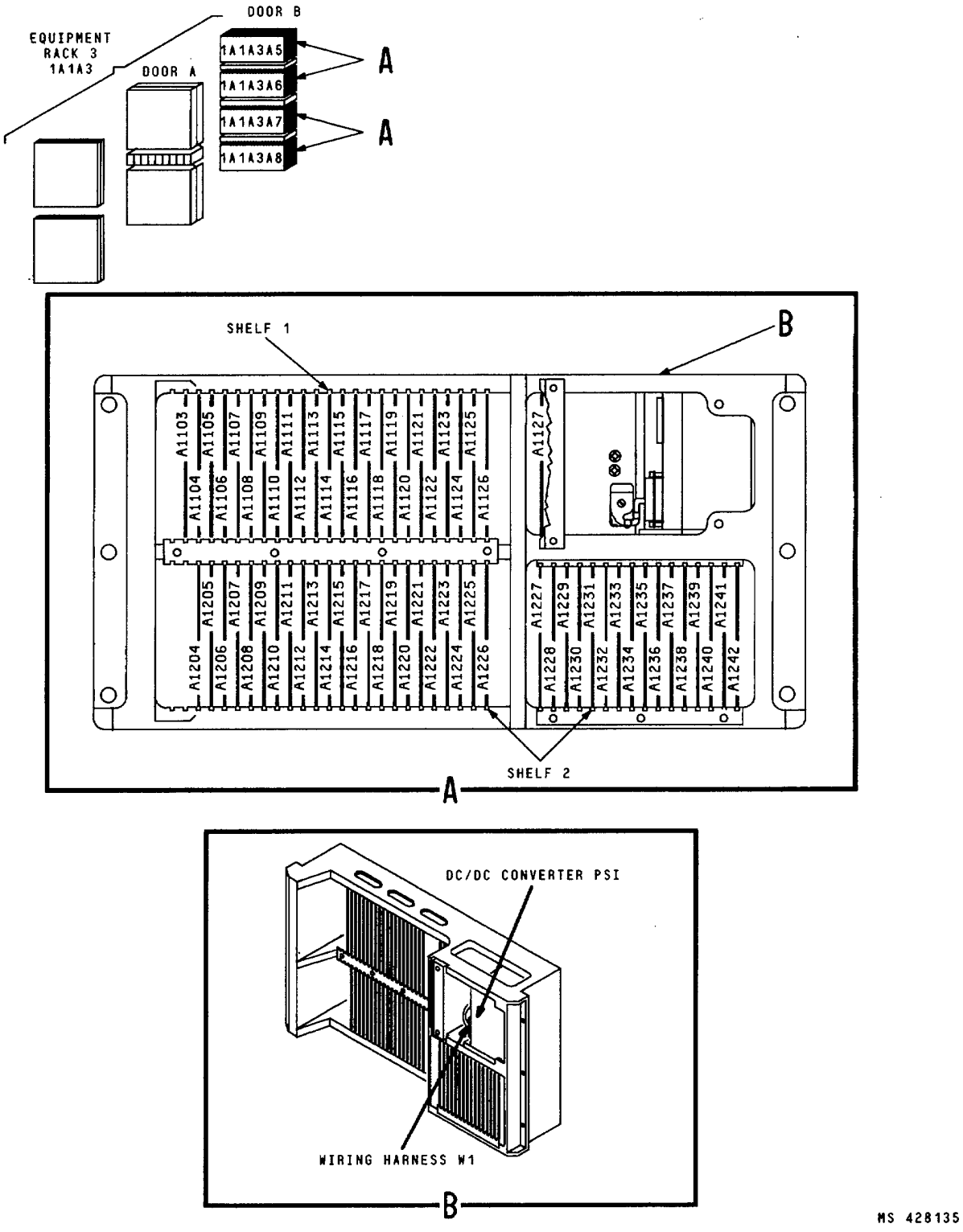

Figure 3-8. 32K Memory Units 1A1A3A5 thru 1A1A3A8, Component Locations

Table 3-3. 32K Memory Units 1A1A3A5 thru 1A1A3A8, Circuit Card Locations

Card slot	Part number	Card type	Color code (zone) 1	2	3	4
		SHELF 1				
A1101	-[1]	Port A I/O (connector)	-	-	-	-
A1102	-[2]	Port B I/O (connector)	-	-	-	-
A1103	149503-100	4-input ac driver/receiver	-	-	503[6]	-
A1104	149503-100	4-input ac driver/receiver	-	-	503[6]	-
A1105	149504-100	Quad 4-input dc driver/ receiver	-	-	504[6]	-
A1106	149504-100	Quad 4-input dc driver/ receiver	-	-	504[6]	-
A1107	149504-100	Quad 4-input de driver/ receiver	-	-	504[6]	-
A1108	149504-100	Quad 4-input dc driver/ receiver	-	-	504[6]	-
A1109	149504-100	Quad 4-input dc driver/ receiver	-	-	504[6]	-
A1110	587106-102	Quad TTL lamp driver	-	-	Blue	-
A1111	587106-102	Quad TTL lamp driver	-	-	Blue	-
A1112	587106-102	Quad TTL lamp driver	-	-	Blue	-
A1113	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1114	10281780	Quad exclusive OR	Brown	Violet	Gray	Black
A1115	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1116	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1117	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1118	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1119	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1120	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1121	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1122	-	Spare	-	-	-	-
A1123	-	Spare	-	-	-	-
A1124	-	Spare	-	-	-	-
A1125	-	Spare	-	-	-	-
A1126	587118-100	1 K-ohm resistor	-	-	118	-
A1127	13143913	Backup control	-	-	-	-
		SHELF 2				
A1201	-[3]	Port C I/O (connector)	-	-	-	-
A1202	-[4]	Port D I/O (connector)	-	-	-	-

See notes at end of table.

Table 3-3. 32K Memory Units 1A1A3A5 thru 1A1A3A8, Circuit Card Locations -Continued

Card slot	Part number	Card type	Color code (zone) 1	2	3	4
A1203	-[5]	Front panel (connector)	-	-	-	-
A1204	149504-100	Quad 4-input dc driver/ receiver	-	-	504[6]	-
A1205	149504-100	Quad 4-input dc driver/ receiver	-	-	504[6]	-
A1206	149504-100	Quad 4-input dc driver/ receiver	-	-	504[6]	-
A1207	149504-100	Quad 4-input dc driver/ receiver	-	-	504[6]	-
A1208	149504-100	Quad 4-input dc driver/ receiver	-	-	504[6]	-
A1209	587106-102	Quad TTL lamp driver	-	-	Blue	-
A1210	587106-102	Quad TTL lamp driver	-	-	Blue	-
A1211	587106-102	Quad TTL lamp driver	-	-	Blue	-
A1212	587119-100	240-ohm resistor	-	-	119	-
A1213	-	Spare	-	-	-	-
A1214	587102-102	Quad 2-input NAND gate		-	Red	-
A1215	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1216	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1217	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1218	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1219	587105-102	Dual D flip-flop	-	-	Green	-
A1220	587105-102	Dual D flip-flop	-	-	Green	-
A1221	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1222	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1223	-	Spare	-	-	-	-
A1224	-	Spare	-		-	-
A1225	10283505	Test set interface	-	-	MTS	-
A1226	-	Spare	-	-	-	-
A1227	-	Spare	-	-	-	-
A1228	13143778	Timing and control	-	-	-	-
A1229	13143777	CMOS storage	-	-	Orange[7]	-
A1230	13143777	CMOS storage	-	-	Orange[7]	-
A1231	13143777	CMOS storage	-	-	Orange[7]	-
A1232	13143777	CMOS storage	-	-	Orange[7]	-
A1233	13143777	CMOS storage	-	-	Orange[7]	-

See notes at end of table.

Table 3-3. 32K Memory Units 1A1A3A5 thru 1A1A3A8, Circuit Card Locations -Continued

Card slot	Part number	Card type	Color code (zone) 1	2	3	4
A1234	13143777	CMOS storage	-	-	Orange[7]	-
A1235	13143777	CMOS storage	-	-	Orange[7]	-
A1236	13143777	CMOS storage	-	-	Orange[7]	-
A1237	13143777	CMOS storage	-	-	Orange[7]	-
A1238	13143777	CMOS storage	-	-	Orange[7]	-
A1239	13143777	CMOS storage	-	-	Orange[7]	-
A1240	-	Spare	-	-	-	-
A1241	-	Spare	-	-	-	-
A1242	-	Spare	-	-	-	-

NOTES:

[1] 1A1A3A5 W327 (P2)
1A1A3A6 W370 (P2)
1A1A3A7 W399 (P2)
1A1A3A8 W453 (P2)

[2] 1A1A3A5 W328 (P2)
1A1A3A6 W371 (P2)
1A1A3A7 W400 (P2)
1A1A3A8 W454 (P2)

[3] 1A1A3A5 W330 (P2)
1A1A3A6 W396 (P2)
1A1A3A7 W424 (P2)
1A1A3A8 W460 (P2)

[4] 1A1A3A5 W331 (P2)
1A1A3A6 W397 (P2)
1A1A3A7 W425 (P2)
1A1A3A8 W461 (P2)

[5] 1A1A3A5 W332 (P2)
1A1A3A6 W398 (P2)
1A1A3A7 W426 (P2)
1A1A3A8 W462 (P2)

[6] 503 and 504 cards have yellow on center of test point edge of circuit card (i.e. not testable by MTS)

[7] 13143777 cards have orange edge to identify CMOS devices; these cards are not testable by MTS and require special handling. Refer to CMOS cautionary notice on page b of this technical manual.

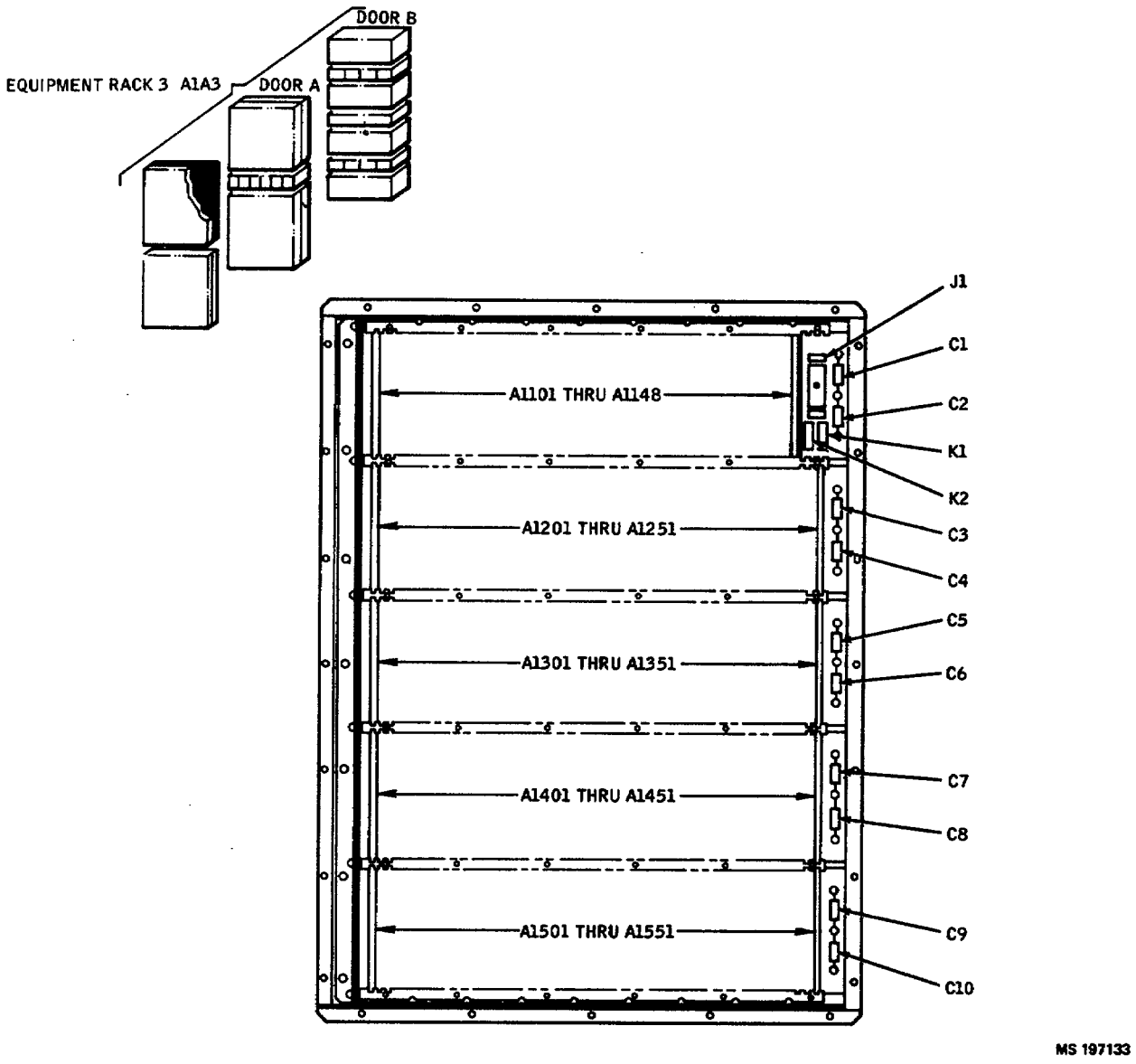

Figure 3-9. Input/Output Unit 1A1A3A1, Component Location

Table 3-4. Input/Output Unit 1A1A3A1, Circuit Card Location

Card slot	Part number	Card type	Color code (zone) 1	2	3	4
		SHELF 1				
A1101	587105-102	Dual D flip-flop	-	-	Green	-
A1102	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1103	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1104	587105-102	Dual D flip-flop	-	-	Green	-
A1105	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1106	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1107	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1108	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1109	587105-102	Dual D flip-flop	-	-	Green	-
A1110	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1111	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1112	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1113	587117-102	Hex inverter	Brown	-	Violet	-
A1114	687102-102	Quad 2-input NAND gate	-	-	Red	-
A1115	587103-102	Triple 3-input NAND gate		-	Orange	-
A1116	587104-102	Dual 4-input NAND gate		-	Yellow	-
A1117	587117-102	Hex inverter	Brown	-	Violet	-
A1118	587103-102	Single 3-input NAND gate	-	-	Orange	-
A1119	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1120	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1121	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1122	-	-	-	-	-	-
A1123	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1124	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1125	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1126	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1127	587117-102	Hex inverter	Brown	-	Violet	-
A1128	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1129	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1130	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1131	-	-	-	-	-	-
A1132	-	-	-	-	-	-

Table 3-4. Input/Output Unit 1A1A3A1, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A1133	587119-100	240-ohm resistor	-	-	-	-
A1134	587128100	Diode/resistor	-	-	-	-
A1135	587128100	Diode/resistor	-	-	-	-
A1136	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1137	587102-102	Quad 2-input NAND gate	-	-	Red	-

Table 3-4. Input/Output Unit 1A1A3A1, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A1138	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1139	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1140	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1141	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1142	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1143	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1144	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1145	587105-102	Dual D flip-flop	-	-	Green	-
A1146	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1147	-		-	-		
A1148	10283505	Test set interface	Orange	Green	Black	Green
		SHELF 2				
A1201	587105-102	Dual D flip-flop	-	-	Green	-
A1202	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1203	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1204	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1205	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1206	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1207	587117-102	Hex inverter	Brown	-	Violet	-
A1208	587105-102	Dual D flip-flop	-	-	Green	-
A1209	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1210	587105-102	Dual D flip-flop	-	-	Green	-
A1211	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1212	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1213	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1214	587105-102	Dual D flip-flop	-	-	Green	-
A1215	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1216	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1217	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1218	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1219	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1220	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1221	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1222	587102-102	Quad 2-input NAND gate	-	-	Red	-

Table 3-4. Input/Output Unit 1A1A3A1, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A1223	587105-102	Dual D flip-flop	-	-	Green	-
A1224	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1225	587108-102	Single 8-input NAND gate		-	Gray	-
A1226	587117-102	Hex inverter	Brown	-	Violet	-
A1227	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1228	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1229	587105-102	Dual D flip-flop	-	-	Green	-
A1230	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1231	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1232	587117-102	Hex inverter	Brown	-	Violet	-
A1233	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1234	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1235	587105-102	Dual D flip-flop	-	-	Green	-
A1236	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1237	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1238	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1239	587117-102	Hex inverter	Brown	-	Violet	-
A1240	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1241	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1242	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1243	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1244	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1245	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1246	587103-102	Triple 3-input NAND gate		-	Orange	-
A1247	587117-102	Hex inverter	Brown	'-	Violet	-
A1248	587119-100	240-ohm resistor	-	-	-	-
A1249	W334	Connector	-	-	-	-
A1250	W335	Connector	-	-	-	-
A1251	W336	Connector	-	-	-	-
		SHELF 3				
A1301	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1302	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1303	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1304	587106-102	Quad 2-input lamp driver	-	-	Blue	-

Table 3-4. Input/Output Unit 1A1A3A1, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A1305	587105-102	Dual D flip-flop	-	-	Green	-
A1306	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1307	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1308	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1309	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1310	587117-102	Hex inverter	Brown	-	Violet	-
A1311	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1312	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1313	587105-102	Dual D flip-flop	-		Green	-
A1314	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1315	587119-100	240-ohm resistor	-	-	-	-
A1316	587100-102	4/8 MHz oscillator	-	-	-	-
A1317	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1318	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1319	587108-102	Single 8-input NAND gate	-	-	Gray	
A1320	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1321	587118-100	1K-ohm resistor	-	-	-	-
A1322	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1323	587105-102	Dual D flip-flop	-	-	Green	-
A1324	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1325	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1326	587010-102	Quad 2-input NAND gate	-	-	Red	-
A1327	587104-102	Dual 4-input NAND gate		-	Yellow	-
A1328	587117-102	Hex inverter	Brown	-	Violet	-
A1329	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1330	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1331	587105-102	Dual D flip-flop	-	-	Green	-
A1332	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1333	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1334	587118-100	1K-ohm resistor	-	-	-	-
A1335	587105-102	Dual D flip-flop	-	-	Green	-
A1336	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1337	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1338	587102-102	Quad 2-input NAND gate	-	-	Red	-

Table 3-4. Input/Output Unit 1A1A3A1, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A1339	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1340	587109-102	Quad 16-bit memory	-	-	White	-
A1341	587109-102	Quad 16-bit memory	-	-	White	-
A1342	587117-102	Hex inverter	Brown	-	Violet	-
A1343	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1344	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1345	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1346	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1347	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1348	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1349	W369	Connector	-	-	-	-
A1350	W524	Connector	-	-	-	-
A1351	W525	Connector	-	-	-	-
		SHELF 4				
A1401		-	-	-	-	-
A1402		-	-	-	-	-
A1403		-	-	-	-	-
A1404	-	-	-	-	-	-
A1405	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1406	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1407	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1408	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1409	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1410	587105-102	Dual D flip-flop	-	-	Green	-
A1411	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1412	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1413	587117-102	Hex inverter	Brown	-	Violet	-
A1414	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1415	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1416	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1417	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1418	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1419	587105-102	Dual D flip-flop	-	-	Green	-
A1420	587108-102	Single 8-input NAND gate	-	-	Gray	-

Table 3-4. Input/Output Unit 1A1A3A1, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A1421	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1422	587119-100	240-ohm resistor	-	-	-	-
A1423	587119-100	240-ohm resistor	-	-	-	-
A1424	587117-102	Hex inverter	Brown	-	Violet	-
A1425	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1426	587124-103	Dc interface 1	Red	-	Yellow	-
A1427	587124-103	Dc interface 1	Red	-	Yellow	-
A1428	587124-103	Dc interface 1	Red	-	Yellow	-
A1429	587124-103	Dc interface 1	Red	-	Yellow	-
A1430	587124-103	Dc interface 1	Red	-	Yellow	-
A1431	587107-102	Ac coupled I/0	-	-	Violet	-
A1432	587124-103	Dc interface 1	Red	-	Yellow	-
A1433	587124-103	Dc interface 1	Red	-	Yellow	-
A1434	587124-103	Dc interface 1	Red	-	Yellow	-
A1435	587124-103	Dc interface 1	Red	-	Yellow	-
A1436	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1437	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1438	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1439	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1440	-	-	-	-	-	-
A1441	587119-100	240-ohm resistor	-	-	-	-
A1442	587119-100	240-ohm resistor	-	-	-	-
A1443	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1444	587128-100	Diode/resistor	-	-	-	-
A1445	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1446	587117-102	Hex inverter	Brown	-	Violet	-
A1447	587105-102	Dual D flip-flop	-	-	Green	-
A1448	-		-	-	-	-
A1449	W374	Connector	-	-	-	-
A1450	W375	Connector	-	-	-	-
A1451	W376	Connector	-	-	-	-
		SHELF 5 (Not Used)				

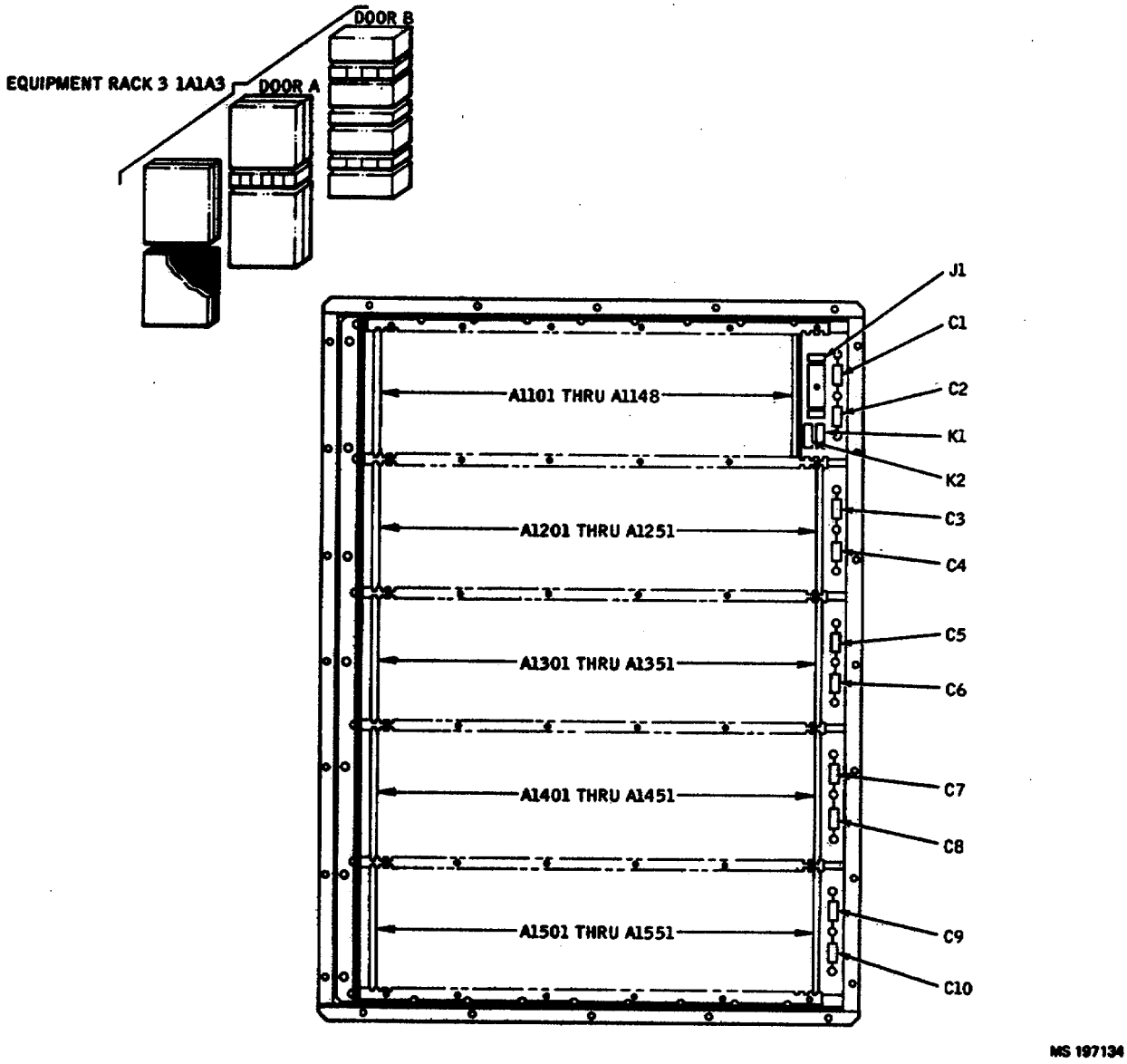

Figure 3-10. Buffer Unit 1A1A3A2, Component Location

Table 3-5. Buffer Unit 1A1A3A2, Circuit Card Location

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
		SHELF 1				
A1101	-	-	-	-	-	-
A1102	-	-	-	-	-	-
A1103	-	-	-	-	-	-
A1104	-	-	-	-	-	-
A1106	-	-	-	-	-	-
A1106	-	-	-	-	-	-
A1107	-	-	-	-	-	-
A1108	-	-	-	-	-	-
A1109	-	-	-	-	-	-
A1110	-	-	-	-	-	-
A1111	-		-	-	-	-
A1112	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1113	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1114	-			-	-	-
A1115	587105-102	Dual D flip-flop	-	-	Green	-
A1116	587105-102	Dual D flip-flop	-	-	Green	-
A1117	587105-102	Dual D flip-flop	-	-	Green	-
A1118	587105-102	Dual D flip-flop	-	-	Green	-
A1119	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1120	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1121	-		-	-	-	-
A1122	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1123	587105-102	Dual D flip-flop	-	-	Green	-
A1124	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1125	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1126	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1127	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1128	687119-102	240-ohm resistor	-	-	-	-
A1129	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1130	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1131	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1132	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1133	-		-	-	-	-
A1134	587104-102	Dual 4-input NAND gate	-	-	Yellow	-

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Table 3-5. Buffer Unit 1A1A3A2, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A1135	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1136	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1137	587105-102	Dual D flip-flop	-	-	Green	-
A1138	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1139	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1140	587105-102	Dual D flip-flop	-	-	Green	-
A1141	-	-	-	-	-	-
A1142	10281694	KPU interface	Brown	Blue	White	Yellow
A1143	10281694	KPU interface	Brown	Blue	White	Yellow
A1144	10281694	KPU interface	Brown	Blue	White	Yellow
A1145	10281694	KPU interface	Brown	Blue	White	Yellow
A1146	10281694	KPU interface	Brown	Blue	White	Yellow
A1147	-	-	-	-	-	-
A1148	10283505	Test set interface	Orange	Green	Black	Green
		SHELF 2				
A1201	587100-102	4/8 MHz oscillator clock	-	-	-	-
A1202	587102-102	Quad 2- input NAND gate	-	-	Red	-
A1203	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1204	587105-102	Dual D flip-flop	-	-	Green	-
A1205	587105-102	Triple 3-input NAND gate	-	-	Green	-
A1206	587103-102	Dual D flip-flop	-	-	Orange	-
A1207	587105-102	Dual D flip-flop	-	-	Green	-
A1208	587105-102	Dual D flip-flop	-	-	Green	-
A1209	587105-102	Dual D flip-flop	-	-	Green	-
A1210	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1211	587102-102	Quad 4-input NAND gate	-	-	Red	-
A1212	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1213	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1214	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1215	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1216	587119-100	240-ohm resistor	-	-	-	-
A1217	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1218	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1219	587105-102	Dual D flip-flop	-	-	Green	-

Table 3-5. Buffer Unit 1A1A3A2, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A1220	587105-102	Dual D flip-flop	-	-	Green	-
A1221	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1222	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1223	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1224	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1225	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1226	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1227	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1228	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1229	587124-103	DC interface I	Red	-	Yellow	-
A1230	587124-103	DC interface 1	Red	-	Yellow	-
A1231	587124-103	DC interface 1	Red	-	Yellow	-
A1232	587124-103	DC interface 1	Red	-	Yellow	-
A1233	587124-103	DC interface 1	Red	-	Yellow	-
A1234	587124-103	DC interface 1	Red	-	Yellow	-
A1235	587124-103	DC interface 1	Red	-	Yellow	-
A1236	587124-103	DC interface 1	Red	-	Yellow	-
A1237	587124-103	DC interface 1	Red	-	Yellow	-
A1238	587119-100	240-ohm resistor	-	-	-	-
A1239	587107-102	AC coupled I/O	-	-	Violet	-
A1240	587107-102	AC coupled I/O	-	-	Violet	-
A1241	587107-102	AC coupled I/O	-	-	Violet	-
A1242	587107-102	AC coupled I/O	-	-	Violet	-
A1243	587107-102	AC coupled I/O	-	-	Violet	-
A1244	587107-102	AC coupled I/O	-	-	Violet	-
A1245	587107-102	AC coupled I/O	-	-	Violet	-
A1246	587139-100	82-ohm resistor	-	-	-	-
A1247	-	-	-	-		-
A1248		-	-	-	-	-
A1249	W468	Connector	-	-	-	-
A1250	W469	Connector	-	-	-	-
A1251	W536	Connector	-	-	-	-

Table 3-5. Buffer Unit 1A1A3A2, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
		SHELF 3				
A1301	587105-102	Dual D flip-flop	-	-	Green	-
A1302	587105-102	Dual D flip-flop	-	-	Green	-
A1303	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1304	-	-	-	-	-	-
A1305	-	-	-	-	-	-
A1306	587104-102	Dual 4-input NAND gate		-	Yellow	-
A1307	587104-102	Dual 4-input NAND gate		-	Yellow	-
A1308	587103-102	Triple 3-input NAND gate		-	Orange	-
A1309	587102-102	Quad 2-input NAND gate		-	Red	-
A1310	587102-102	Quad 2-input NAND gate		-	Red	-
A1311	587102-102	Quad 2-input NAND gate		-	Red	-
A1312		-		-	-	-
A1313	587102-102	Quad 2-input NAND gate		-	Red	-
A1314	587104-102	Dual 4-input NAND gate		-	Yellow	-
A1315	587103-102	Triple 3-input NAND gate		-	Orange	-
A1316	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1317	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1318	587119-100	240-ohm resistor	-	-	-	-
A1319	-	-	-	-	-	-
A1320	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1321	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1322	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1323	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1324	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1325	587119-100	240-ohm resistor	-	-	-	-
A1326	-	-	-	-	-	-
A1327	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1328	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1329	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1330	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1331	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1332	587119-100	240-ohm resistor	-	-	-	-
A1333	-	-	-	-	-	-

Table 3-5. Buffer Unit 1A1A3A2, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A1334	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1335	587107-102	AC coupled I/O	-	-	Violet	-
A1336	587107-102	AC coupled I/O	-	-	Violet	-
A1337	587107-102	AC coupled I/O	-	-	Violet	-
A1338	587107-102	AC coupled I/O	-	-	Violet	-
A1339	587107-102	AC coupled I/O	-	-	Violet	-
A1340	587107-102	AC coupled I/O	-	-	Violet	-
A1341	587107-102	AC coupled I/O	-	-	Violet	-
A1342	587107-102	AC coupled I/O	-	-	Violet	-
A1343	587107-102	AC coupled I/O	-	-	Violet	-
A1344	587107-102	AC coupled I/O	-	-	Violet	-
A1345	587107-102	AC coupled I/O	-	-	Violet	-
A1346	587139-100	82-ohm resistor	-	-	-	-
A1347	-	-	-	-	-	-
A1348	-	-	-	-	-	-
A1349	W433	Connector	-	-	-	-
A1350	W524	Connector	-	-	-	-
A1351	W525	Connector	-	-	-	-
		SHELF 4				
A1401	-	-	-	-	-	-
A1402	-	-	-	-	-	-
A1403	-	-	-	-	-	-
A1404	-	-	-	-	-	-
A1405	-	-				
A1406	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1407	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1408	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1409	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1410	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1411	587119-100	240-ohm resistor	-	-	-	-
A1412	-		-	-	-	-
A1413	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1414	587104-102	Quad 4-input NAND gate	-	-	Yellow	-
A1415	587103-102	Triple 3-input NAND gate	-	-	Orange	-

Table 3-4. Input/Output Unit 1A1A3A1, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A1416	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1417	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1418	587119-100	240-ohm resistor	-	-	-	-
A1419	-	-	-	-	-	-
A1420	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1421	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1422	587103-102	Triple 3-input NAND gate		-	Orange	-
A1423	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1424	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1425	587119-100	240-ohm resistor	-	-	-	-
A1426	-	-	-	-	-	-
A1427	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1428	587104-102	Dual 4-input NAND gate		-	Yellow	-
A1429	587103-102	Triple 3-input NAND gate		-	Orange	-
A1430	587102-102	Quad 2-input NAND gate		-	Red	-
A1431	587106-102	Quad 2-input lamp driver		-	Blue	-
A1432	587119-100	240-ohm resistor	-	-	-	-
A1433	-	-	-	-	-	-
A1434	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1435	587107-102	AC coupled I/O	-	-	Violet	-
A1436	587107-102	AC coupled I/O	-	-	Violet	-
A1437	587107-102	AC coupled I/O	-	-	Violet	-
A1438	587107-102	AC coupled I/O	-	-	Violet	-
A1439	587107-102	AC coupled I/O	-	-	Violet	-
A1440	587107-102	AC coupled I/O	-	-	Violet	-
A1441	587107-102	AC coupled I/O	-	-	Violet	-
A1442	587107-102	AC coupled I/O	-	-	Violet	-
A1443	587107-102	AC coupled I/O	-	-	Violet	-
A1444	587107-102	AC coupled I/O	-	-	Violet	-
A1445	587107-102	AC coupled I/O	-	-	Violet	-
A1446	587139-100	82-ohm resistor	-	-	-	-
A1447	-	-	-	-	-	-
A1448	-	-	-	-	-	-
A1449	W457	Connector	-		-	-

Table 3-5. Buffer Unit 1A1A3A2, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A1450	W458	Connector	-	-	-	-
A1451	W459	Connector	-	-	-	-
		SHELF 5				
A1502	-	-	-	-	-	-
A1503	-	-	-	-	-	-
A1504	-	-	-	-	-	-
A1505	-	-	-	-	-	-
A1506	-	-	-	-	-	-
A1507	-	-	-	-	-	-
A1508	-	-	-	-	-	-
A1509	-	-	-	-	-	-
A1510	-		-	-	-	-
A1511	587119-100	240-ohm resistor	-	-	-	-
A1512	-	-	-	-	-	-
A1513	-	-	-	-	-	-
A1514	-	-	-	-	-	-
A1515	-	-	-	-	-	-
A1516	-	-	-	-	-	-
A1517	-	-	-	-	-	-
A1518	587119-100	-240-ohm resistor	-	-	-	-
A1519	-	-	-	-	-	-
A1520	-	-	-	-	-	-
A1521	-	-	-	-	-	-
A1522	-	-	-	-	-	-
A1523	-	-	-	-	-	-
A1524	-	-	-	-	-	-
A1525	587119-100	240-ohm resistor	-	-	-	-
A1526	-	-	-	-	-	-
A1527	-	-	-	-	-	-
A1528	-	-	-	-	-	-
A1529	-	-	-	-	-	-
A1530	-	-	-	-	-	-
A1531	-	-	-	-	-	-

Table 3-5. Buffer Unit 1A1A3A2, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A1532	587119-100	240-ohm resistor				
A1533	-	-	-	-	-	-
A1534	-	-	-	-	-	-
A1535	-	-	-	-	-	-
A1536	-	-	-	-	-	-
A1537	-	-	-	-	-	-
A1538	-	-	-	-	-	-
A1539	-	-	-	-	-	-
A1540	-	-	-	-	-	-
A1541	-	-	-	-	-	-
A1542	-	-	-	-	-	-
A1543	-	-	-	-	-	-
A1544	-	-	-	-	-	-
A1545	-	-	-	-	-	-
A1546	-	-	-	-	-	-
A1547	587128-100	Diode/resistor	-	-	-	-
A1548	587119-100	240-ohm resistor	-	-	-	-
A1549	W463	Connector	-	-	-	-
A1550	W464	Connector	-	-	-	-
A1551	W465	Connector	-	-	-	-

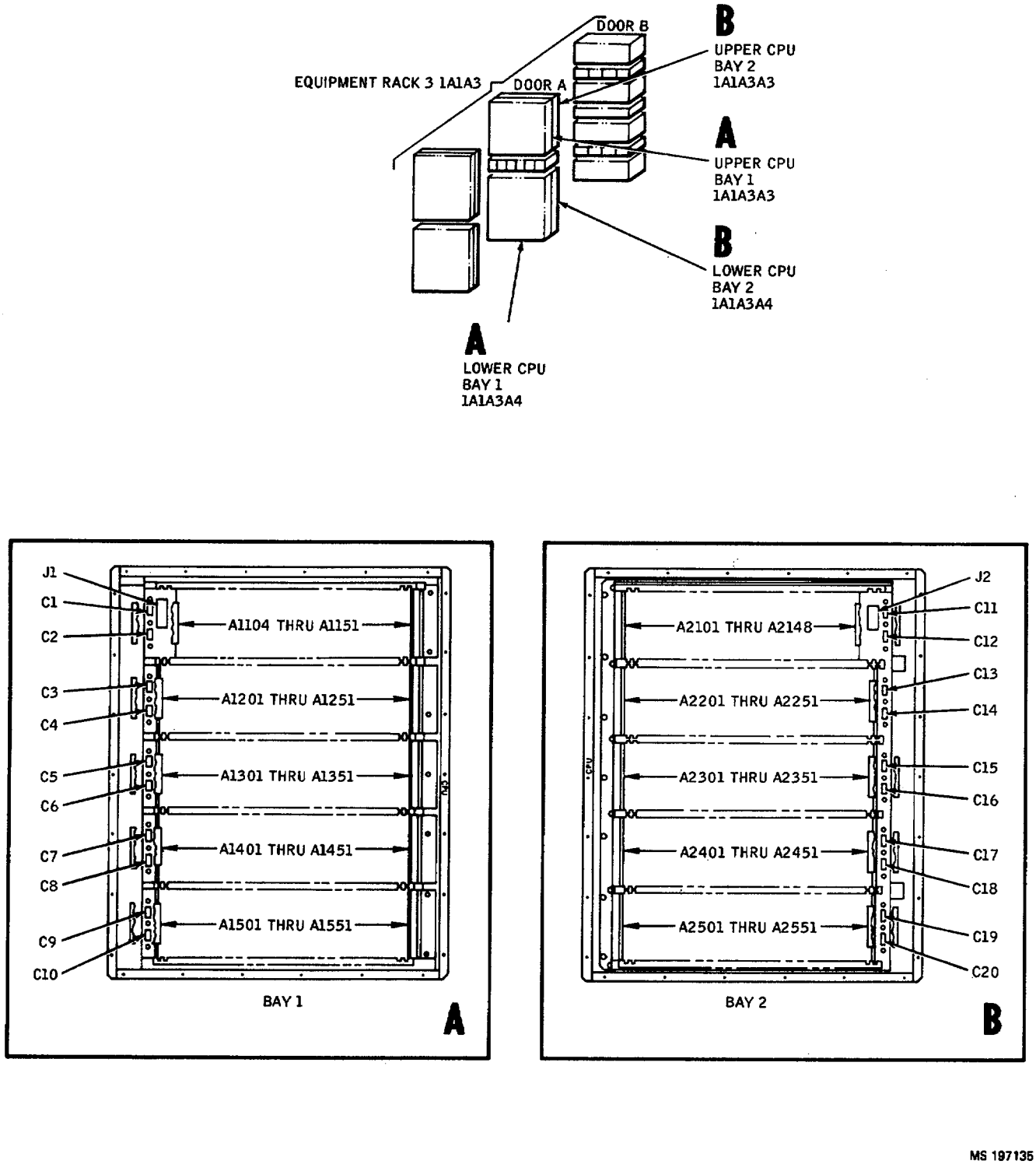


Figure 3-11. Upper Central Processor Unit 1A1A3A3 and Lower Central Processor Unit 1A1A3A4, Component Location

Table 3-6. Upper Central Processor Unit 1A1A3A3 and Lower Central Processor Unit 1A1A3A4, Circuit Card Location

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
		BAY 1-SHELF 1				
A1104	W338	Connector	-	-	-	-
A1105	W337	Connector	-	-	-	-
A1106	-	-	-	-	-	-
A1107	10283505	Test set interface	Orange	Green	Black	Green
A1108	-	-	-	-	-	-
A1109		-	-	-	-	-
A1110	-	-	-	-	-	-
A1111	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1112	587105-102	Dual D flip-flop	-	-	Green	-
A1113	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1114	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1115	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1116	587105-102	Dual D flip-flop	-	-	Green	-
A1117	587105-102	Dual D flip-flop	-	-	Green	-
A1118	587105-102	Dual D flip-flop	-	-	Green	-
A1119	-	-	-	-	-	-
A1120	-	-	-	-	-	-
A1121	587118-100	1 K-ohm resistor	-	-	-	-
A1122	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1123	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1124	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1125	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1126	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1127	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1128	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1129	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1130	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1131	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1132	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1133	-	-	-	-	-	-
A1134		-	-	-	-	-
A1135	587118-100	1 K-ohm resistor		-		-
A1136	587104-102	Dual 4-input NAND gate	-	-	Yellow	-

Table 3-6. Upper Central Processor Unit 1A1A3A3 and Lower Central Processor Unit 1A1A3A4, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A1137	587105-102	Dual D flip-flop	-	-	Green	-
A1138	587105-102	Dual D flip-flop	-	-	Green	-
A1139	587105-102	Dual D flip-flop	-	-	Green	-
A1140	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1141	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1142	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1143	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1144	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1145	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1146	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1147	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1148	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1149	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1150	587102-102	Quad 2- Input NAND gate	-	-	Red	-
A1151	587102-102	Quad 2-input NAND gate	-	-	Red	-
		BAY 1-SHELF 2				
A1201	W340	Connector	-		-	-
A1202	W339	Connector	-		-	-
A1203	-	-	-		-	-
A1204	-	-	-		-	-
A1205	-	-	-	-	-	-
A1206	-	-	-	-	-	-
A1207		-	-	-	-	-
A1208	-	-	-	-	-	-
A1209	587118-100	1 K-ohm resistor	-	-	-	-
A1210	587105-102	Dual D flip-flop	-	-	Green	-
A1211	587105-102	Dual D flip-flop	-	-	Green	-
A1212	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1213	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1214	587110-102	Adder	-	-	Black	-
A1215	587130-102	Adder/decoder	-	-	-	-
A1216	587110-102	Adder	-	-	Black	-

Table 3-6. Upper Central Processor Unit 1A1A3A3 and Lower Central Processor Unit 1A1A3A4, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A1217	587130-102	Adder/decoder	-	-	-	-
A1218	587130-102	Adder/decoder	-	-	-	-
A1219	587130-102	Adder/decoder	-	-	-	-
A1220	587130-102	Adder/decoder	-	-	-	-
A1221	587130-102	Adder/decoder	-	-	-	-
A1222	587119-100	240-ohm resistor	-	-	-	-
A1223	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1224	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1225	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1226	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1227	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1228	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1229	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1230	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1231	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1232	-	-	-	-	-	-
A1233	-	-	-	-	-	-
A1234	587118-100	1 K-ohm resistor	-	-	-	-
A1235	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1236	587105-102	Dual D flip-flop	-	-	Green	-
A1237	587105-102	Dual D flip-flop	-	-	Green	-
A1238	587105-102	Dual D flip-flop	-	-	Green	-
A1239	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1240	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1241	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1242	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1243	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1244	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1245	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1246	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1247	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1248	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1249	587103-102	Triple 3-input NAND gate	-	-	Orange	-

Table 3-6. Upper Central Processor Unit 1A1A3A3 and Lower Central Processor Unit 1A1A3A4, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A1250	-	-	-	-	-	-
A1251	-	-	-	-	-	-
		BAY 1-SHELF 3				
A1301	W378	Connector	-	-	-	-
A1302	W377	Connector	-	-	-	-
A3A1303	W368	Connector	-	-	-	-
A4A1303	W432	Connector	-	-	-	-
A1304	-	-	-	-	-	-
A1305	-	-	-	-	-	-
A1306	-	-	-	-	-	-
A1307	-	-	-	-	-	-
A1308	-	-	-	-	-	-
A1309	-	-	-	-	-	-
A1310	587118-100	1 K-ohm resistor	-	-	-	-
A1311	587119-100	240-ohm resistor	-	-	-	-
A1312	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1313	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1314	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1315	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1316	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1317	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1318	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1319	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1320	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1321	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1322	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1323	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1324	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1325	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1326	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1327	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1328	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1329	587106-102	Quad 2-input lamp driver	-	-	Blue	-

Table 3-6. Upper Central Processor Unit 1A1A3A3 and Lower Central Processor Unit 1A1A3A4, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A1330	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1331	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1332	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1333	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1334	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A1335	587102-102	Quad 2-input lamp driver	-	-	Red	-
A1336	587102-102	Quad 2-input lamp driver	-	-	Red	-
A1337	587102-102	Quad 2-input lamp driver	-	-	Red	-
A1338	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1339	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1340	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1341	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1342	587119-100	240-ohm resistor	-	-	-	-
A1343	587118-100	1 K-ohm resistor	-	-	-	-
A1344	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1345	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1346	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1347	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1348	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1349	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1350	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1351	-		-	-	-	-
		BAY 1-SHELF 4				
A1401	W380	Connector	-	-	-	-
A1402	W379	Connector	-		-	-
A3A1403	W373	Connector	-	-	-	-
A4A1403	W456	Connector	-	-	-	-
A1404	587119-100	240-ohm resistor	-	-	-	-
A1405	587107-102	AC coupled I/O	-	-	Violet-	
A1406	587124-103	DC interface 1	Red	-	Yellow	-
A1407	587124-103	DC interface 1	Red	-	Yellow	-
A1408	587124-103	DC interface 1	Red	-	Yellow	-

Table 3-6. Upper Central Processor Unit 1A1A3A3 and Lower Central Processor Unit 1A1A3A4, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A1409	587124-103	DC interface 1	Red	-	Yellow	-
A1410	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1411	587105-102	Dual D flip-flop	-	-	Green	-
A1412	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1413	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1414	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1415	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1416	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1417	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1418	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1419	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1420	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1421	587105-102	Dual D flip-flop	-	-	Green	-
A1422	587105-102	Dual D flip-flop	-	-	Green	-
A1423	587105-102	Dual D flip-flop	-	-	Green	-
A1424	587105-102	Dual D flip-flop	-	-	Green	-
A1425	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1426	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1427	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1428	587109-102	Quad 16-bit memory	-	-	White	-
A1429	587109-102	Quad 16-bit memory	-	-	White	-
A1430	587118-100	1 K-ohm resistor	-	-	-	-
A1431	587109-102	Quad 16-bit memory	-	-	White	-
A1432	587109-102	Quad 16-bit memory	-	-	White	-
A1433	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1434	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1435	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1436	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1437	587109-102	Quad 16-bit memory	-	-	White	-
A1438	587109-102	Quad 16-bit memory	-	-	White	-
A1439	587118-100	1 K-ohm resistor	-	-	-	-
A1440	587109-102	Quad 16-bit memory	-	-	White	-
A1441	587109-102	Quad 16-bit memory	-	-	White	-

Table 3-6. Upper Central Processor Unit 1A1A3A3 and Lower Central Processor Unit 1A1A3A4, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A1442	587109-102	Quad 16-bit memory	-	-	White	-
A1443	587109-102	Quad 16-bit memory	-	-	White	-
A1444	587118-100	1 K-ohm resistor	-	-	-	-
A1445	587109-102	Quad 16-bit memory	-	-	White	-
A1446	587109-102	Quad 16-bit memory	-	-	White	-
A1447	587102-102	Quad 2-input NAND gate		-	Red	-
A1448	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1449	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1450	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1451	587102-102	Quad 2-input NAND gate	-	-	Red	-
		BAY 1-SHELF 5				
A1501	W403	Connector	-	-	-	-
A1502	W402	Connector	-	-	-	-
A1503	-	-	-	-	-	
A1504	587119-100	240-ohm resistor	-	-	-	-
A1505	587124-103	DC interface 1	Red	-	Yellow	-
A1506	587124-103	DC interface 1	Red	-	Yellow	-
A1507	587124-103	DC interface 1	Red	-	Yellow	-
A1508	587124-103	DC interface 1	Red	-	Yellow	-
A1509	587124-103	DC interface 1	Red	-	Yellow	-
A1510	587124-103	DC interface 1	Red	-	Yellow	-
A1511	587102-102	Quad 2-input NAND gate	-		Red	-
A1512	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1513	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1514	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1515	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1516	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1517	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1518	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1519	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1520	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1521	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1522	587102-102	Quad 2-input NAND gate	-	-	Red	-

Table 3-6. Upper Central Processor Unit 1A1A3A3 and Lower Central Processor Unit 1A1A3A4, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A1523	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1524	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1525	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1526	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1527	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1528	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1529	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1530	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1531	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1532	587105-102	Dual D flip-flop	-	-	Green	-
A1533	587105-102	Dual D flip-flop	-	-	Green	-
A1534	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1535	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1536	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1537	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1538	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1539	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1540	587108-102	Single 8-input NAND gate	-	-	Gray	-
A1541	-		-	-	-	-
A1542	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1543	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1544	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1545	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1546	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1547	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1548	587102-102	Quad 2-input NAND gate	-	-	Red	-
A1549	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A1550	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A1551	587105-102	Dual D flip-flop	-	-	Green	-
		BAY 2-SHELF 1				
A2101	-		-	-	-	-
A2102	-		-	-	-	-
A2103	587108-102	Single 8-input NAND gate	-	-	Gray	-

Table 3-6. Upper Central Processor Unit 1A1A3A3 and Lower Central Processor Unit 1A1A3A4, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A2104	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2105	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2106	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2107	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2108	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2109	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2110	587108102	Single 8-input NAND gate	-	-	Gray	-
A2111	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2112	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2113	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2114	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2115	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2116	587105-102	Dual D flip-flop	-	-	Green	-
A2117	587105-102	Dual D flip-flop	-	-	Green	-
A2118	-	-	-	-	-	-
A2119	587119-100	240-ohm resistor	-	-	-	-
A2120	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2121	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2122	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2123	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2124	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2125	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2126	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2127	587103-102	Triple 3-input NAND gate		-	Orange	-
A2128	587105-102	Dual D flip-flop	-	-	Green	-
A2129	587105-102	Dual D flip-flop	-	-	Green	-
A2130	587118-100	1 K-ohm resistor	-	-	-	-
A2131	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2132	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2133	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2134	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2135	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2136	587118100	1 K-ohm resistor	-	-	-	-

Table 3-6. Upper Central Processor Unit 1A1A3A3 and Lower Central Processor Unit 1A1A3A4, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A2137						
A2138	-	-	-	-	-	-
A2139	-	-	-	-	-	-
A2140	-	-	-	-	-	-
A2141	-	-	-	-	-	-
A2142	-	-	-	-	-	-
A2143	-	-	-	-	-	-
A2144	-	-	-	-	-	-
A2145	-	-	-	-	-	
A3A2146	W329	Connector	-	-	-	-
A4A2146	W401	Connector	-		-	-
A2147	W337	Connector	-		-	-
A2148	W338	Connector	-		-	-
		BAY 2-SHELF 2				
A2201	-		-	-	-	-
A2202	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2203	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2204	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2205	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2206	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2207	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2208	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2209	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2210	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2211	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2212	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2213	587105-102	Dual D flip-flop	-	-	Green	-
A2214	587118-100	1 K-ohm resistor	-	-	-	-
A2215	587105-102	Dual D flip-flop	-	-	Green	-
A2216	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2217	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2218	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2219	587108-102	Single 8-input NAND gate	-	-	Gray	-

Table 3-6. Upper Central Processor Unit 1A1A3A3 and Lower Central Processor Unit 1A1A3A4, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A2220	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2221	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2222	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2223	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2224	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2225	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2226	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2227	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2228	-	-	-	-	-	-
A2229	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2230	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2231	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2232	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2233	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2234	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2235	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2236	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2237	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2238	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2239	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2240	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2241	587108102	Single 8-input NAND gate	-	-	Gray	-
A2242	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2243	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2244	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2245	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2246	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2247	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2248	587108-102	Single 8-input NAND gate	-	-	Gray	-
A3A2249	W333	Connector	-	-	-	-
A4A2249	W427	Connector	-	-	-	-
A2250	W339	Connector	-	-	-	-
A2251	W340	Connector	-		-	-

Table 3-6. Upper Central Processor Unit 1A1A3A3 and Lower Central Processor Unit 1A1A3A4, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
		BAY 2-SHELF 3				
A2301	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2302	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2303	-	-	-	-	-	-
A2304	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2305	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2306	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2307	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2308	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2309	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2310	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2311	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2312	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2313	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2314	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2315	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2316	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2317	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2318	587119-100	240-ohm resistor	-	-	-	-
A2319	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2320	587119-100	240-ohm resistor	-	-	-	-
A2321	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2322	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2323	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2324	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2325	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A2326	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A2327	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A2328	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A2329	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A2330	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A2331	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A2332	587106-102	Quad 2-input lamp driver	-	-	Blue	-
A2333	587106-102	Quad 2-input lamp driver	-	-	Blue	-

Table 3-6. Upper Central Processor Unit 1A1A3A3 and Lower Central Processor Unit 1A1A3A4, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A2334	587118-100	1 K-ohm resistor	-	-	-	-
A2335	587128-100	Diode/resistor	-	-	-	-
A2336	587118-100	1 K-ohm resistor	-	-	-	-
A2337	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2338	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2339	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2340	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2341	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2342	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2343	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2344	587105-102	Dual D flip-flop	-	-	Green	-
A2345	587100-102	4/8 MHz oscillator	-	-	-	-
A2346	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2347	-		-		-	-
A2348	587102-102	Quad 2-input NAND gate	-	-	Red	-
A3A2349	W367	Connector	-		-	-
A4A2349	W431	Connector	-	-	-	-
A2350	W377	Connector	-	-	-	-
A2351	W378	Connector	-	-	-	-
		BAY 2-SHELF 4				
A2401	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2402	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2403			-	-	-	-
A2404	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2405	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2406	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2407	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2408	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2409	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2410	587102-102	Quad 2-input NAND ate	-	-	Red	-
A2411	587105-102	Dual D flip-flop	-	-	Green	-
A2412	587105-102	Dual D flip-flop	-	-	Green	-
A2413	587118-100	1 K-ohm resistor	-	-	-	-

Table 3-6. Upper Central Processor Unit 1A1A3A3 and Lower Central Processor Unit 1A1A3A4, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A2414	-	-	-	-	-	-
A2415	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2416	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2417	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2418	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2419	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2420	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2421	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2422	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2434	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2424	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2425	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2426	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2427	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2428	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2429	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2430.	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2431	587105-102	Dual D flip-flop	-	-	Green	-
A2432	587105-102	Dual D flip-flop	-	-	Green	-
A2433	587118-100	1 K-ohm resistor	-	-	-	-
A2434	-	-	-	-	-	-
A2435	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2436	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2437	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2438	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2439	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2440	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2441	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2442	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2443	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2444	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2445	587102-102	Quad 2-input NAND gate	-	-	Red	-

Table 3-6. Upper Central Processor Unit 1A1A3A3 and Lower Central Processor Unit 1A1A3A4, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A2446	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2447	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2448	587108-102	Single 8-input NAND gate	-	-	Gray	-
A3A2449	W372	Connector	-	-	-	-
A4A2449	W455	Connector	-	-	-	-
A2450	W379	Connector	-	-	-	-
A2451	W380	Connector	-	-	-	-
		BAY 2-SHELF 5				
A2501	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2502	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2503	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2504	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2505	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2506	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2507	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2508	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2509	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2510	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2511	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2512	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2513	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2514	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2515	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2516	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2517	587105-102	Dual D flip-flop	-	-	Green	-
A2518	587105-102	Dual D flip-flop	-	-	Green	-
A2519	587105-102	Dual D flip-flop	-	-	Green	-
A2520	587118-100	1 K-ohm resistor	-	-	-	-
A2521	-	-	-	-	-	-
A2522	587118-100	1 K-ohm resistor	-	-	-	-
A2523	587105-102	Dual D flip-flop	-	-	Green	-
A2524	587105-102	Dual D flip-flop	-	-	Green	-
A2525	587104-102	Dual 4-input NAND gate		-	Yellow	-

Table 3-6. Upper Central Processor Unit 1A1A3A3 and Lower Central Processor Unit 1A1A3A4, Circuit Card Location -Continued

Card Slot	Part number	Card type	Color code (zone) 1	2	3	4
A2526	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2527	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2528	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2529	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2530	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2531	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2532	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2533	-	-	-	-	-	-
A2534	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2535	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2536	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2537	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2538	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2539	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2540	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2541	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2542	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2543	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2544	587103-102	Triple 3-input NAND gate	-	-	Orange	-
A2545	587102-102	Quad 2-input NAND gate	-	-	Red	-
A2546	587104-102	Dual 4-input NAND gate	-	-	Yellow	-
A2547	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2548	587108-102	Single 8-input NAND gate	-	-	Gray	-
A2549	-	-	-	-	-	-
A2550	W402	Connector	-	-	-	-
A2551	W403	Connector	-	-	-	-

Section III. FAULT ISOLATION AND TROUBLESHOOTING

3-12. General. This section provides FI and troubleshooting information and data for the ADP equipment. Before initiating FI or troubleshooting procedures, refer to the troubleshooting section of Overall System Maintenance Manual TM 9-1430-655-20-1 to determine if the trouble is external to the ADP equipment or is a transient fault. Refer also to Fault Catalog TM 9-1430-655-20-2 for FI and troubleshooting procedures using the Module Test Set (MTS) and card substitution.

3-13. Procedural Guidelines. Fault detection is a function of the computer software, built-in test equipment, and personal observations. When an abnormal condition occurs in the system, identify all of the indications, determine if a fault exists and, if so, which unit is at fault. Refer to TM 9-1430-655-20-1 for system fault isolation. The ADP equipment FI flow chart provides logical procedures to isolate the fault. If an FI program is indicated, execute the FI program according to the procedures contained in TM 9-1430-655-20-1. The FI program causes an error stop number to be displayed on the ADP status and control panel with amplifying data printed out on the KPU. The error stop number is a 6-digit number that corresponds to possible faulty cards listed in the fault catalog. If the malfunction remains uncorrected, standard troubleshooting procedures must be performed to correct the malfunction. Operator observation and documentation instructions determine which path to follow for FI. Table 3-7 defines the flow chart symbology used.

a. System Fault Indications. Several types of indications are provided for the operator: fault indicators, KPU message outputs, equipment indicators, display messages, and inoperative system functions. Analysis of system fault indications will lead maintenance personnel to the system FI flow chart. The system FI flow chart will then lead to the appropriate unit FI chart.

b. System FI Program. The FI program is initiated by performing procedures contained in TM 9-1430-655-20-1. If a fault exists, an error stop number is displayed on the ADP status and control panel or printed out on the KPU. This error stop number corresponds to a number located in Fault Catalog TM 9-1430-655-20-2.

c. Fault. Catalog. The fault catalog provides a list of possible faulty cards and modules corresponding to each error stop number. Instructions are given to either test the cards in or out of the system using the MTS, or to check faulty cards/modules by the substitution method.

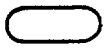
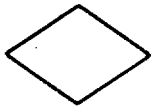
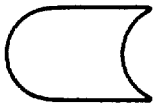
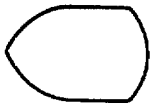
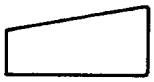
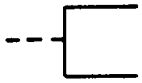
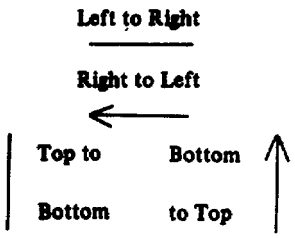
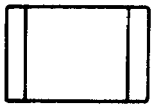
*d. MTS***.** The MTS performs continuity and functional tests of circuit cards. Through use of the fault catalog, the error stop number identifies a group of circuit cards associated with the fault symptom. Maintenance personnel then perform card test procedures contained in TM 91430-655-20-9 to isolate the fault to a defective circuit card. The flow charts provide procedures to verify that the fault is corrected. If the fault still exists, FI is accomplished using standard troubleshooting procedures.

e. Standard. T1oubleshooting Procedures. A fault in the backplane wiring or other areas not isolated by the MTS must be traced to its source using the system wire lists and an oscilloscope or multimeter. To determine the correct area of a wiring fault, an evaluation of the MTS test indications must be performed using TM 9-1430-655-20-9. The FI flow chart should be used as a guide to simplify manual troubleshooting procedures. When signal tracing fails to isolate the fault, logical circuit card or unit substitution should be performed.

f. System FI Flow Chart. The system FI flow chart contained in TM 9-1430-655-20-1 enables maintenance personnel to isolate to a major unit as defined by the status indications. The system FI flow chart (fig. 3-12) directs maintenance personnel to the appropriate unit FI flow chart.

g. ADP Unit Fl Flow Chart. The unit FI flow charts (fig. 3-13) provide maintenance personnel with a series of logical procedures to isolate a fault. The unit FI flow chart directs maintenance personnel to perform additional procedures such as FI program execution procedures, circuit card test procedures, circuit card substitution, realinements, and interface checks. When performing these procedures, additional instructions may be printed out on the KPU. Table 3-8 provides a list of lamp test indications called out in figure 3-13. Table 3-9 identifies buffer unit card functional groups (also called out in figure 3-13).

Table 3-7. Flow Chart Symbology

Symbol	Definition
	Terminal Symbol—represents a terminal point in the flow chart such as start, stop, halt, delay, or interrupt. Data may enter or leave at this point.
	Connector Symbol—represents a junction in a line of flow. A set of two is used to represent a continued flow direction when the flow is broken by chart limitations.
	Manual Operation Symbol—represents any off-line function or process geared to human speed.
	Decision Symbol—represents a decision on switching type operation that determines which of a number of paths is to be followed.
	On-Line Storage Symbol—represents an I/O function utilizing mass information storage that can be accessed on-line.
	Display Symbol—represents an I/O function in which the information is displayed for human use at the time of processing (i.e., indicators, printouts, plots, etc.).
	Manual Input Symbol—represents an I/O function in which information is manually entered through on-line keyboards, switch settings, card readers, pushbuttons, etc.
	Document Symbol—represents an I/O function in which the medium is a document.
	Magnetic Tape Symbol—represents an I/O function in which the medium is magnetic tape.
	Annotation Symbol—represents the addition of descriptive comments or explanatory notes. A broken line may be drawn to the left or to the right and connected to the flow line at its most meaningful point.
	Process Symbol—represents the processing functions in which the process of executing a defined operation or group of operations results in a change in value, form, or location of information.
	Flow Line Symbols—represent the direction of information or operational flow.
	Predefined Process Symbol—represents a named process consisting of one or more operations or program steps specified elsewhere (not this flow chart).

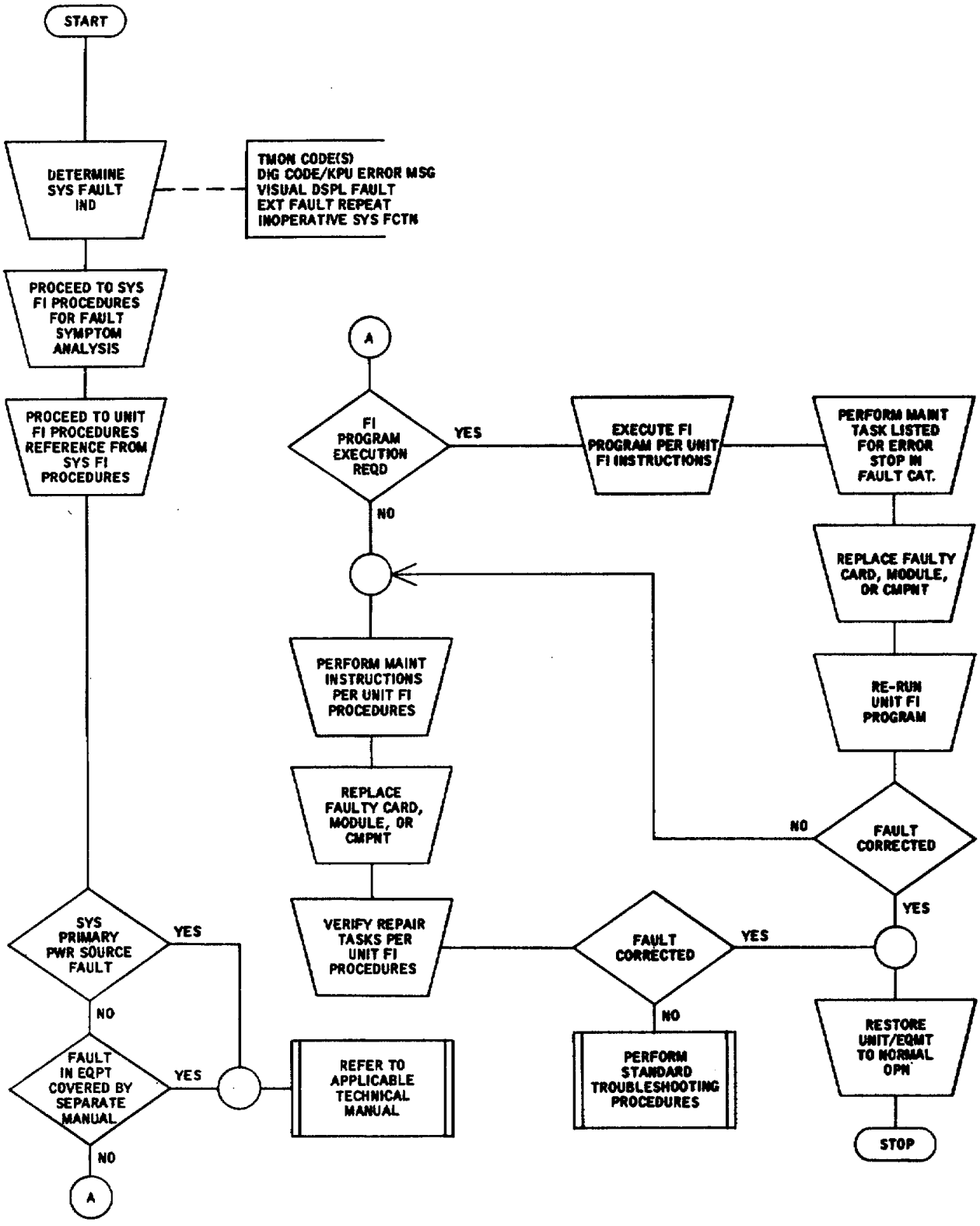
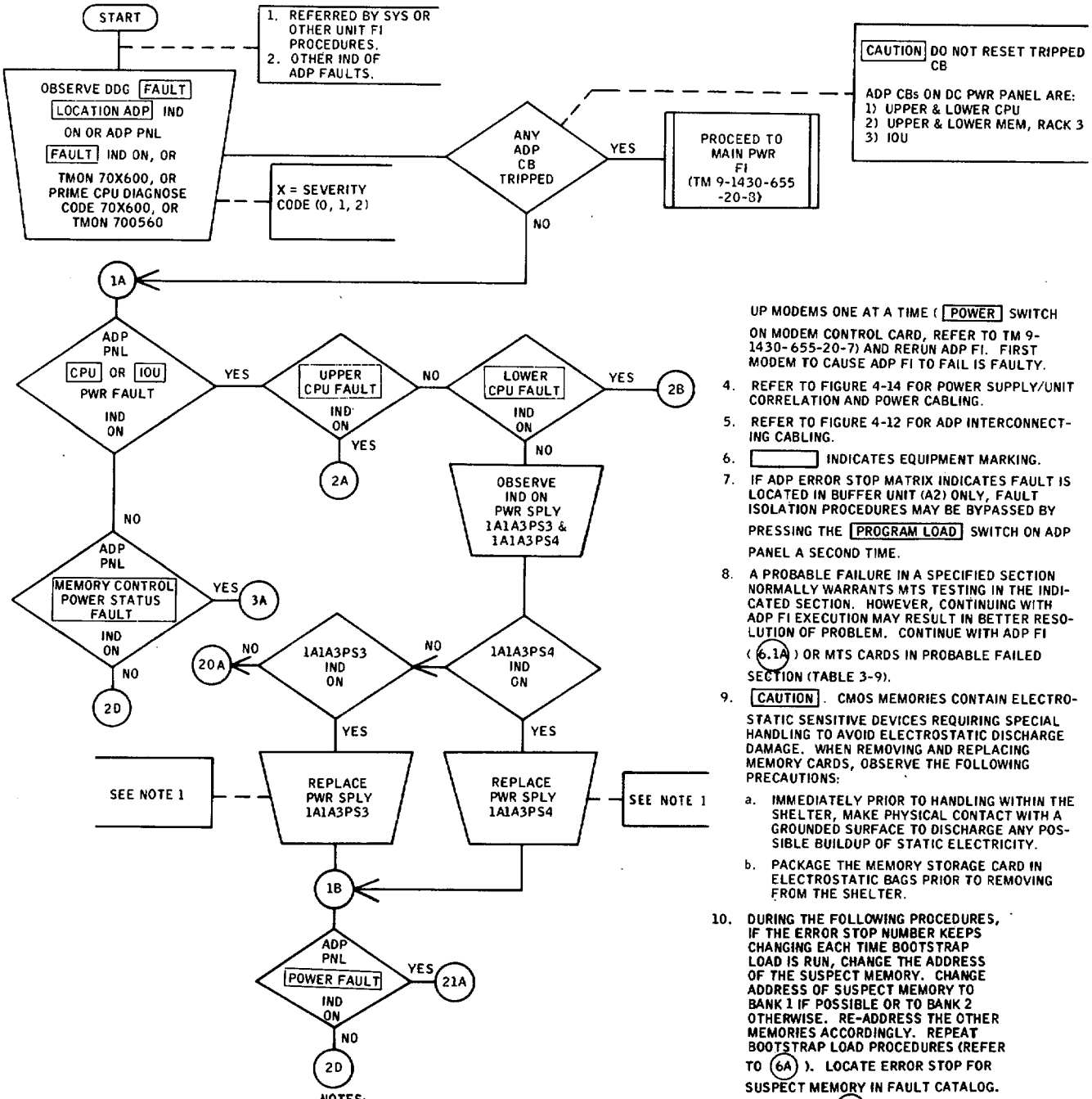


Figure 3-12. AN/TSQ-73 Troubleshooting Sequence



NOTES:

1. IF UNIT POWER SUPPLY DOES NOT TURN OFF WHEN REMOVING UNIT POWER, REFER TO (19A)
2. REFERENCES TO ERROR STOP MATRIX AND FAULT CATALOG REFER TO TM 9-1430-655-20-2.
3. IN CASE OF RIE FAILURE (AND UNABLE TO RUN RIE FI PROGRAM) TEST REPORT BUFFER AND I/O SECTIONS FIRST (REFER TO FUNCTIONAL UNIT CARD DATA TABLE TM 9-1430-655-20-3). IN CASE OF DATA COMM FAILURE, DETERMINE FIRST WHICH MODEM HAS FAILED BY POWERING UP MODEMS ONE AT A TIME (POWER SWITCH ON MODEM CONTROL CARD, REFER TO TM 9-1430-655-20-7) AND RERUN ADP FI. FIRST MODEM TO CAUSE ADP FI TO FAIL IS FAULTY.
4. REFER TO FIGURE 4-14 FOR POWER SUPPLY/UNIT CORRELATION AND POWER CABLING.
5. REFER TO FIGURE 4-12 FOR ADP INTERCONNECTING CABLING.
6. [ ] INDICATES EQUIPMENT MARKING.
7. IF ADP ERROR STOP MATRIX INDICATES FAULT IS LOCATED IN BUFFER UNIT (A2) ONLY, FAULT ISOLATION PROCEDURES MAY BE BYPASSED BY PRESSING THE PROGRAM LOAD SWITCH ON ADP PANEL A SECOND TIME.
8. A PROBABLE FAILURE IN A SPECIFIED SECTION NORMALLY WARRANTS MTS TESTING IN THE INDICATED SECTION. HOWEVER, CONTINUING WITH ADP FI EXECUTION MAY RESULT IN BETTER RESOLUTION OF PROBLEM. CONTINUE WITH ADP FI ((6.1A)) OR MTS CARDS IN PROBABLE FAILED SECTION (TABLE 3-9).
9. CAUTION . CMOS MEMORIES CONTAIN ELECTROSTATIC SENSITIVE DEVICES REQUIRING SPECIAL HANDLING TO AVOID ELECTROSTATIC DISCHARGE DAMAGE. WHEN REMOVING AND REPLACING MEMORY CARDS, OBSERVE THE FOLLOWING PRECAUTIONS:
   a. IMMEDIATELY PRIOR TO HANDLING WITHIN THE SHELTER, MAKE PHYSICAL CONTACT WITH A GROUNDED SURFACE TO DISCHARGE ANY POSSIBLE BUILDUP OF STATIC ELECTRICITY.
   b. PACKAGE THE MEMORY STORAGE CARD IN ELECTROSTATIC BAGS PRIOR TO REMOVING FROM THE SHELTER.
10. DURING THE FOLLOWING PROCEDURES, IF THE ERROR STOP NUMBER KEEPS CHANGING EACH TIME BOOTSTRAP LOAD IS RUN, CHANGE THE ADDRESS OF THE SUSPECT MEMORY. CHANGE ADDRESS OF SUSPECT MEMORY TO BANK 1 IF POSSIBLE OR TO BANK 2 OTHERWISE. RE-ADDRESS THE OTHER MEMORIES ACCORDINGLY. REPEAT BOOTSTRAP LOAD PROCEDURES (REFER TO (6A)). LOCATE ERROR STOP FOR SUSPECT MEMORY IN FAULT CATALOG. PROCEED TO (12A) .
    IF AFTER RE-ADDRESSING THE SUSPECT MEMORY THE ERROR STOP NUMBER CONTINUES TO CHANGE EACH TIME BOOTSTRAP LOAD IS RUN, SELECT THE MOST PROBABLE ERROR STOP. LOCATE THIS ERROR STOP IN THE FAULT CATALOG UNDER THE SECTION FOR THE SUSPECT MEMORY. THEN PROCEED TO (12A) AND PERFORM THE ACTIONS SPECIFIED FOR THIS ERROR STOP.

MS 428136

Figure 3-13. ADP Fault Isolation Flow chart (Sheet 1 of 37)

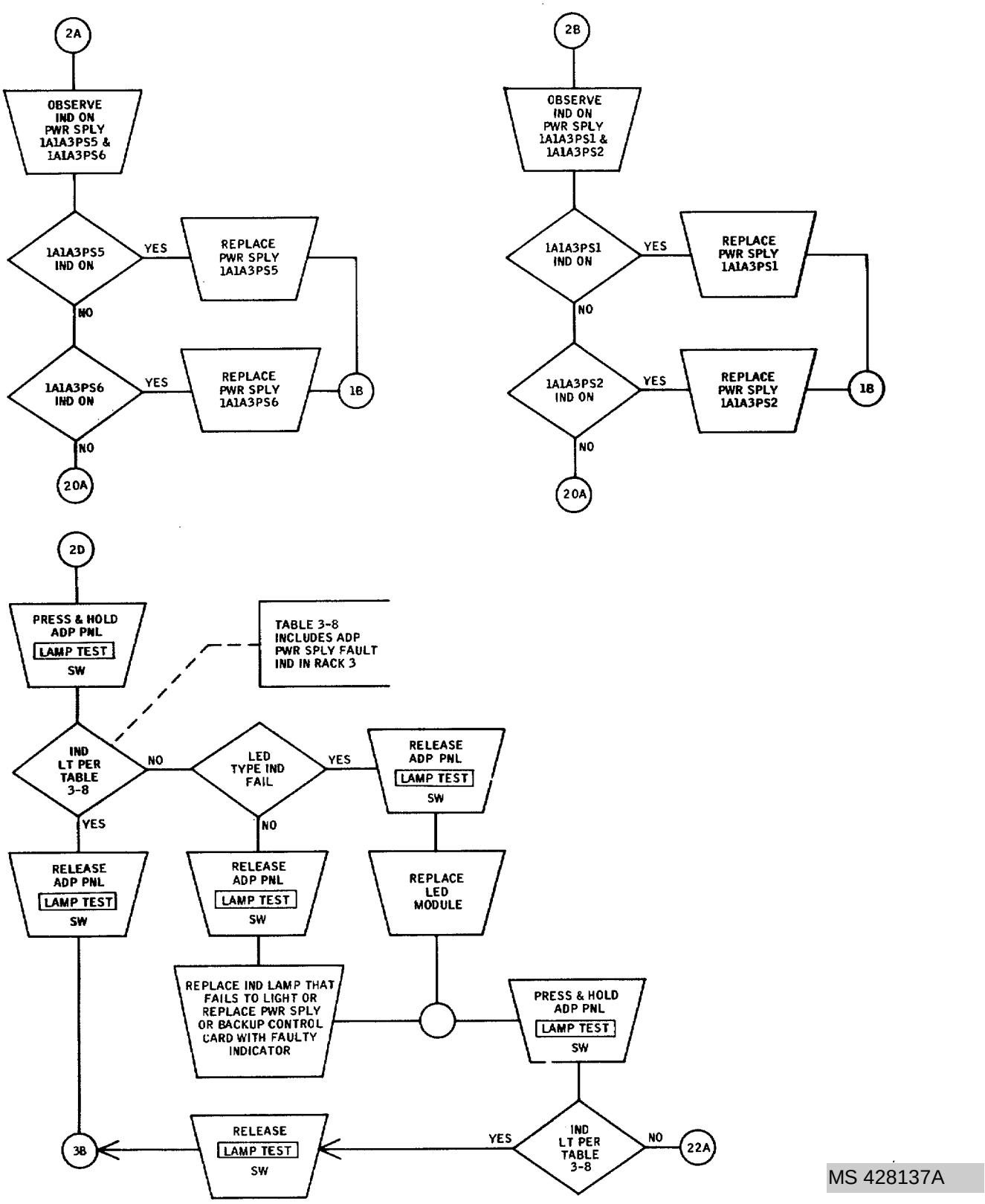


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 2 of 37)

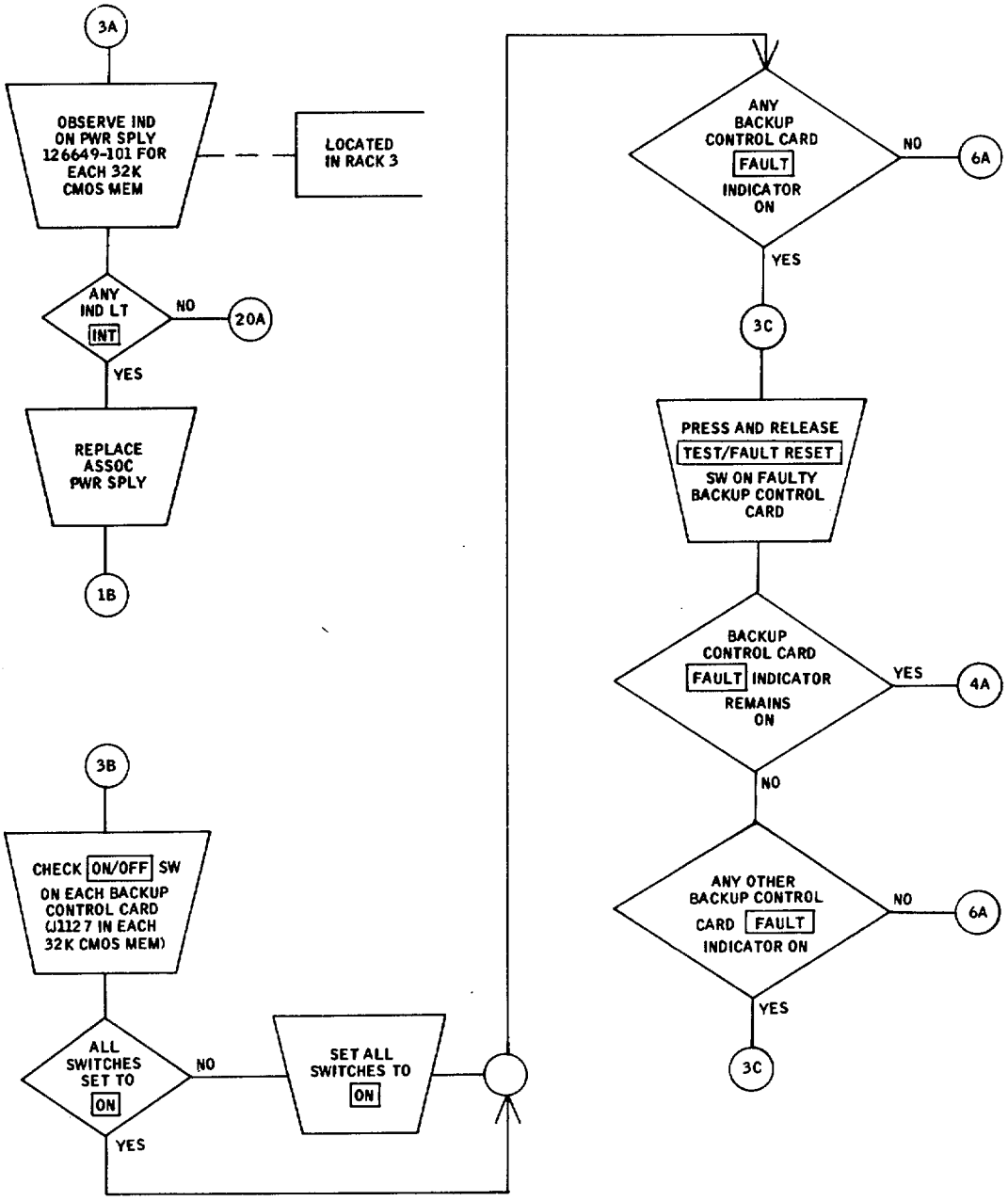


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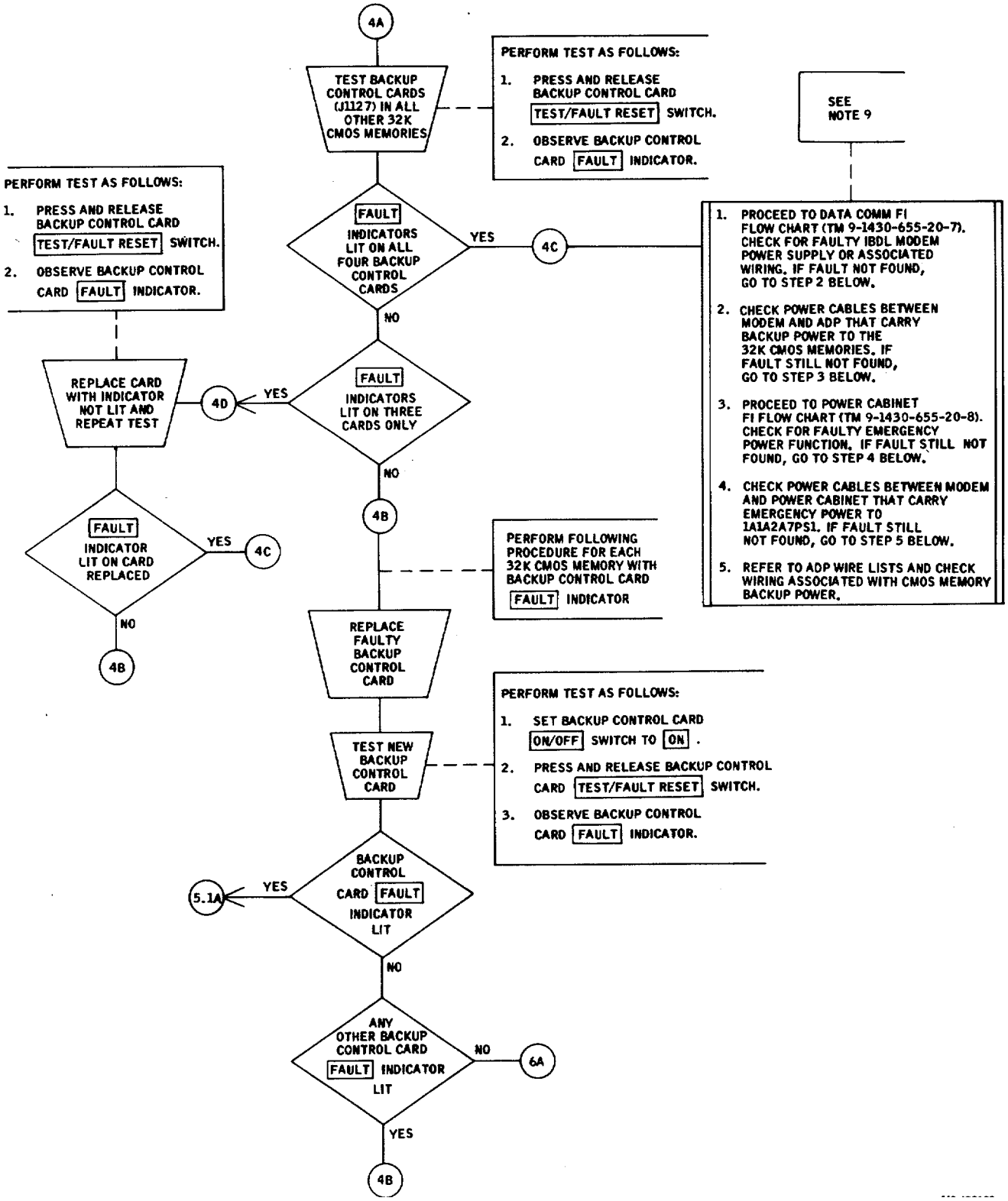
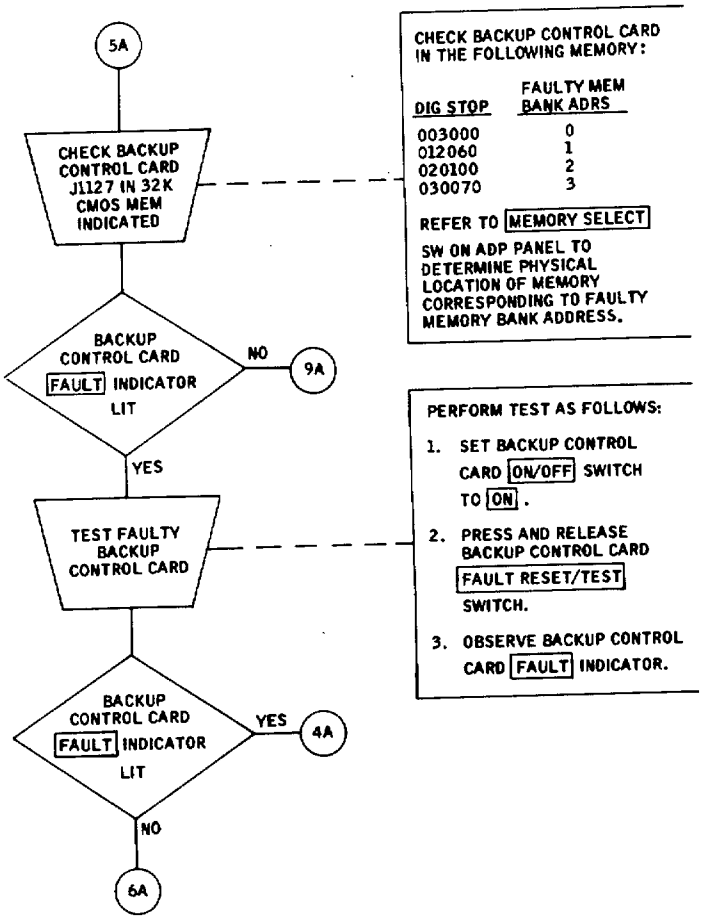
Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 3 of 37)



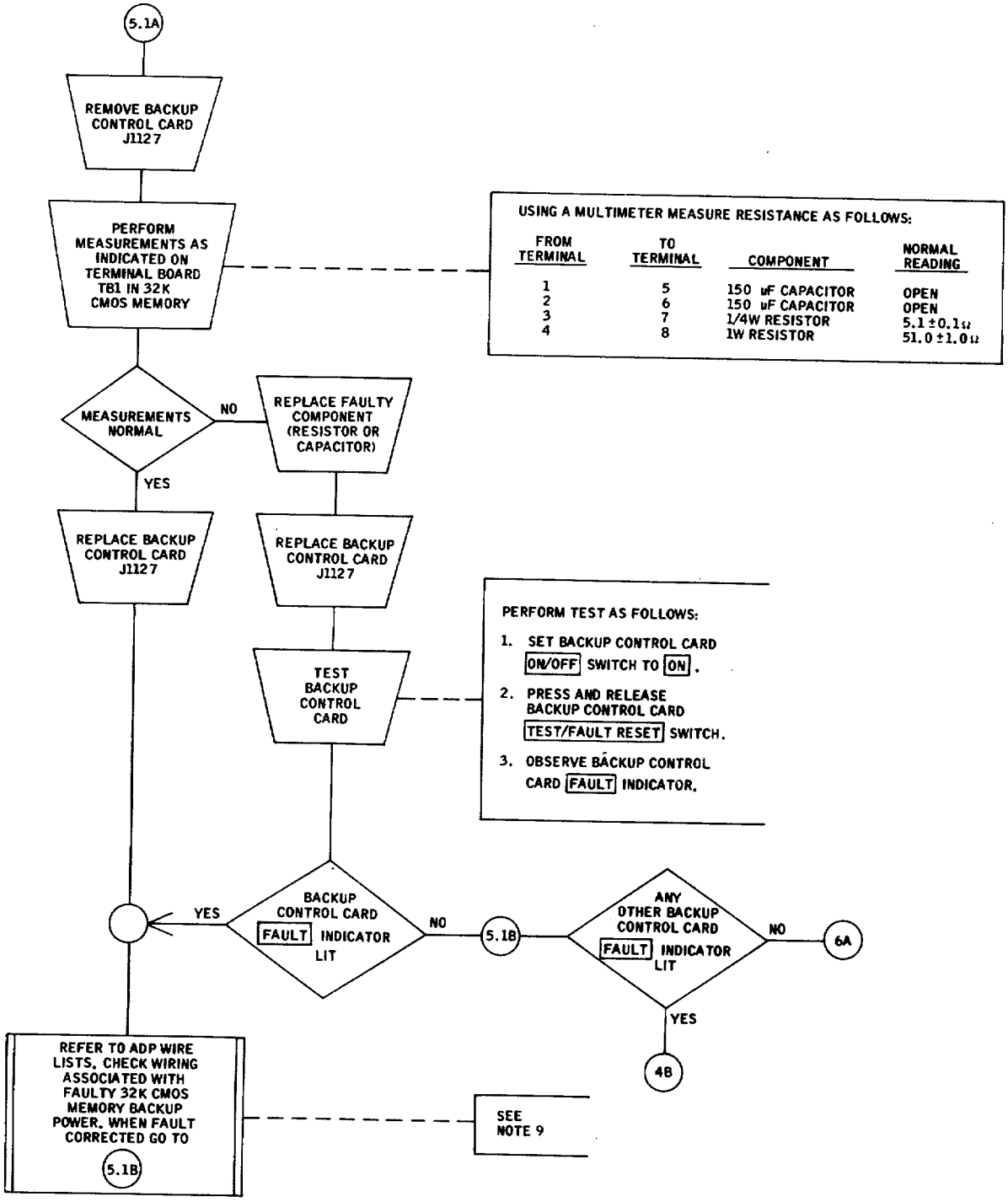
MS 428139

Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 4 of 37)



MS 428140

Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 5 of 37)



MS 428141

Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 5.1 of 37)

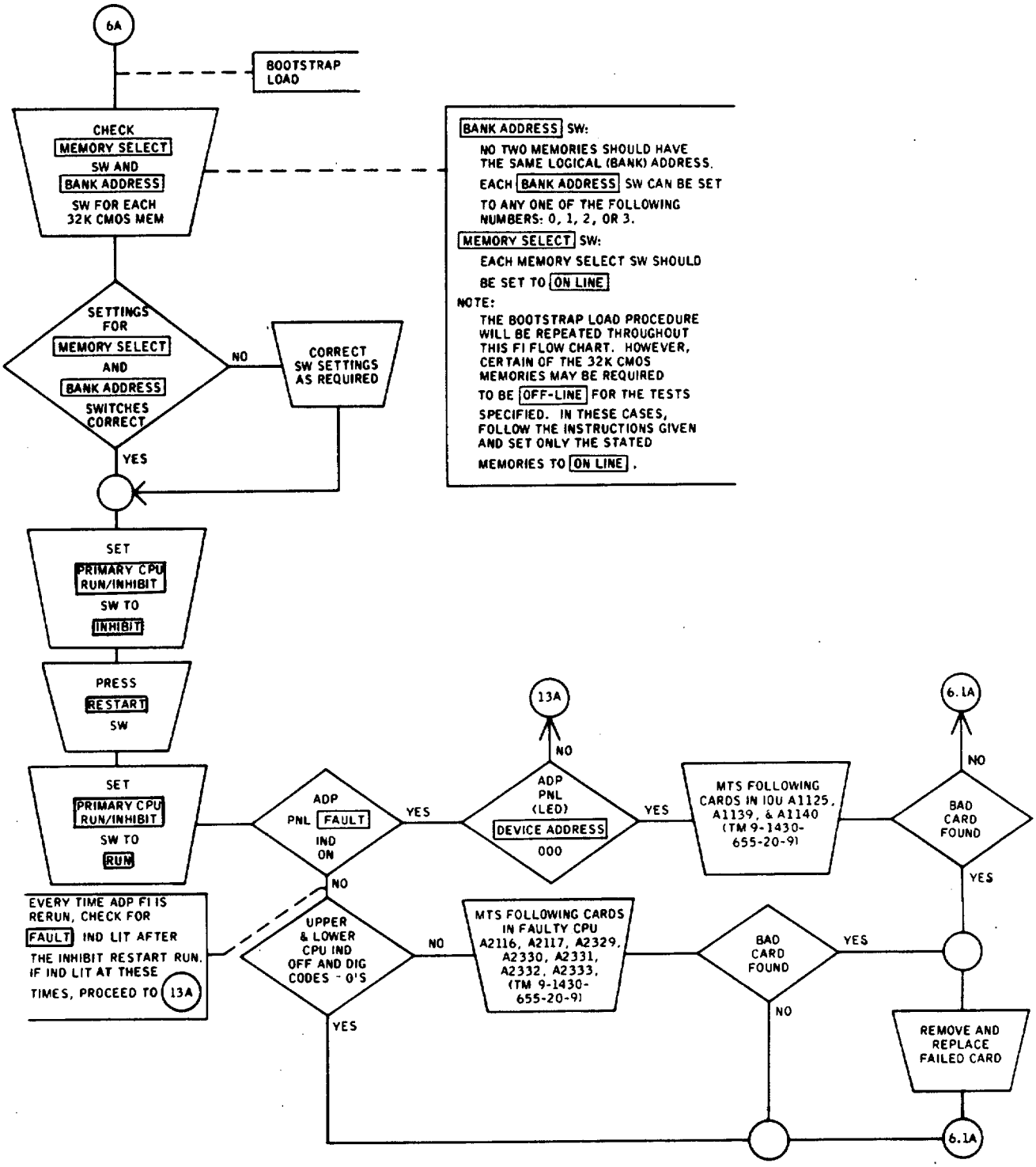
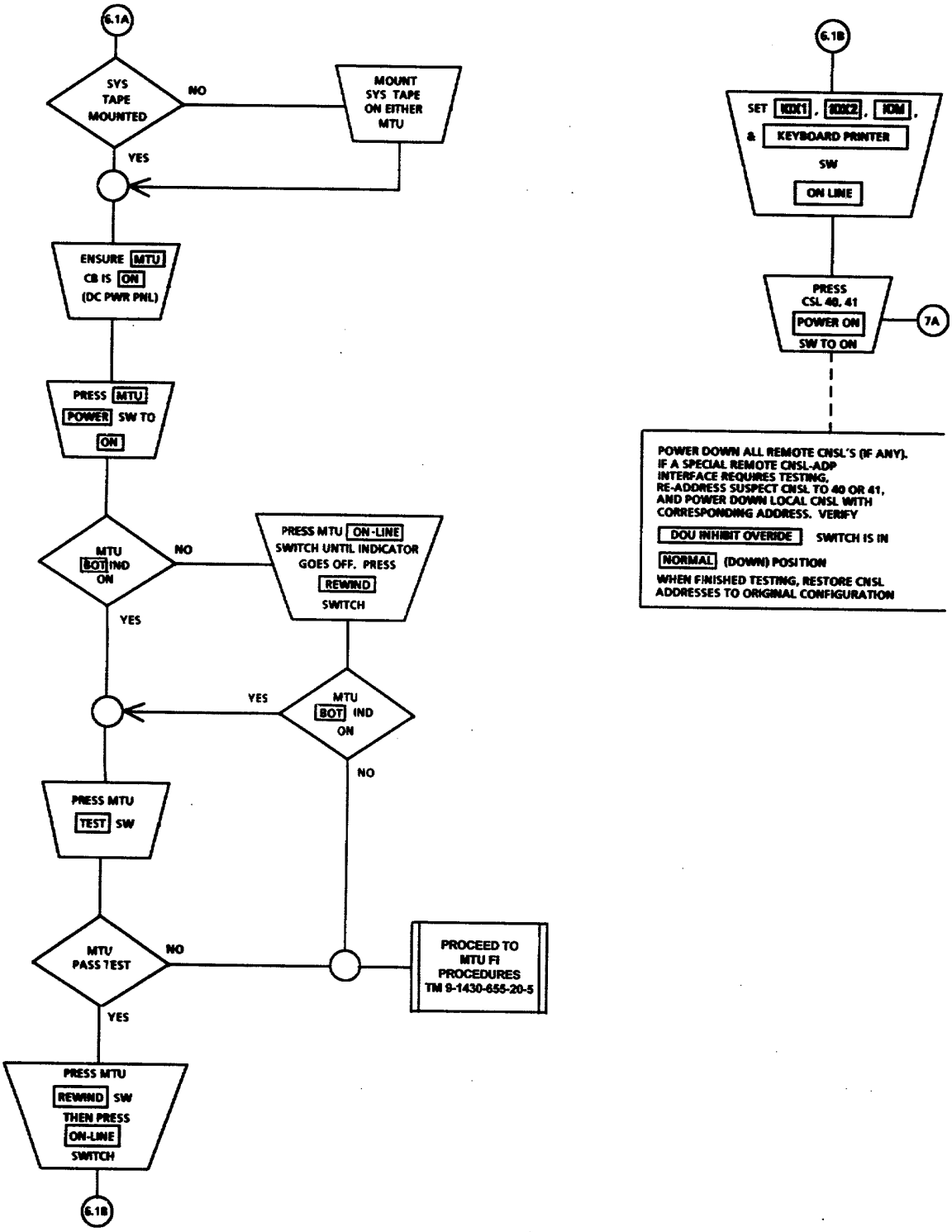


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 6 of 37)



MS 012922B

Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 6.1 of 37)

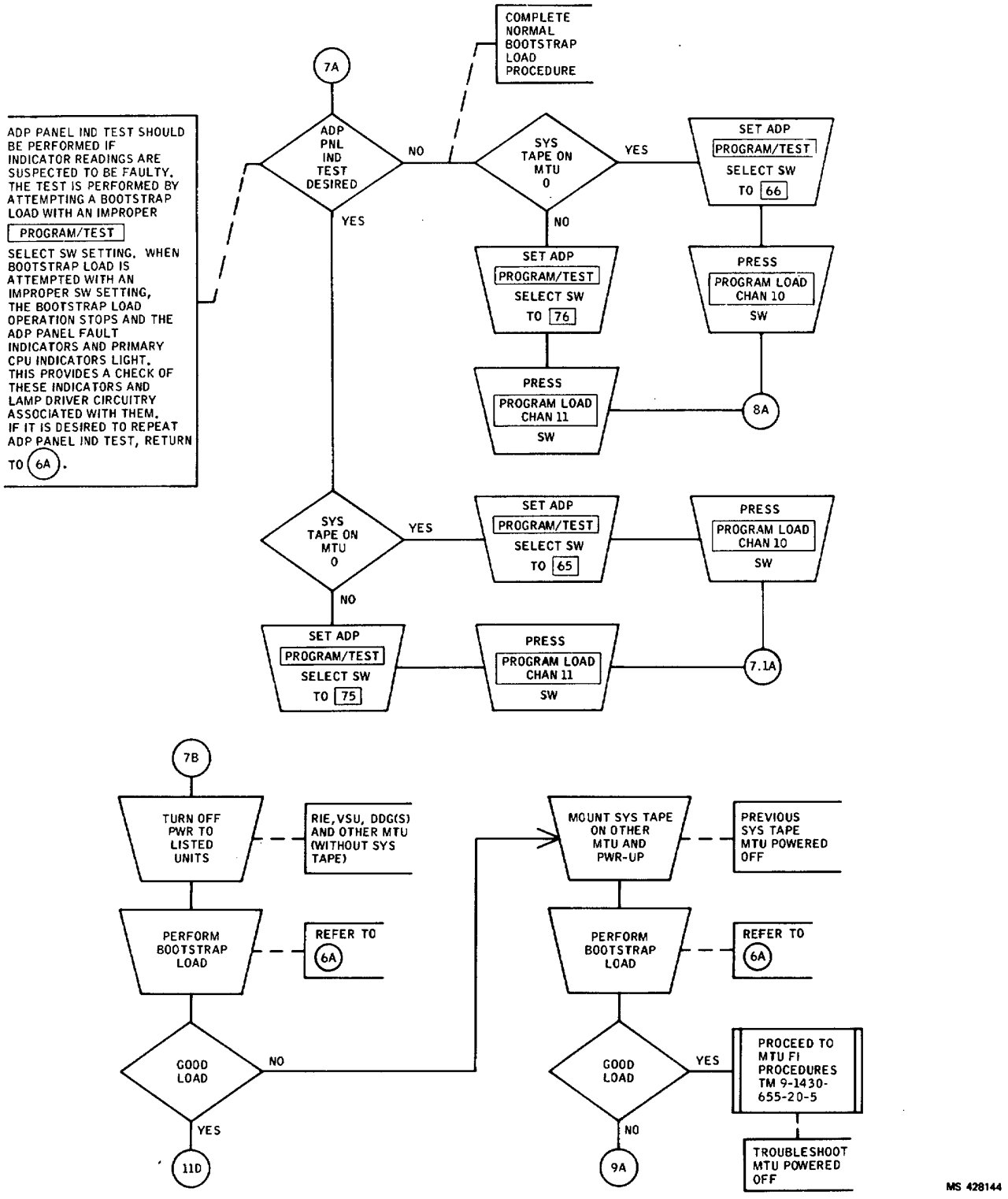
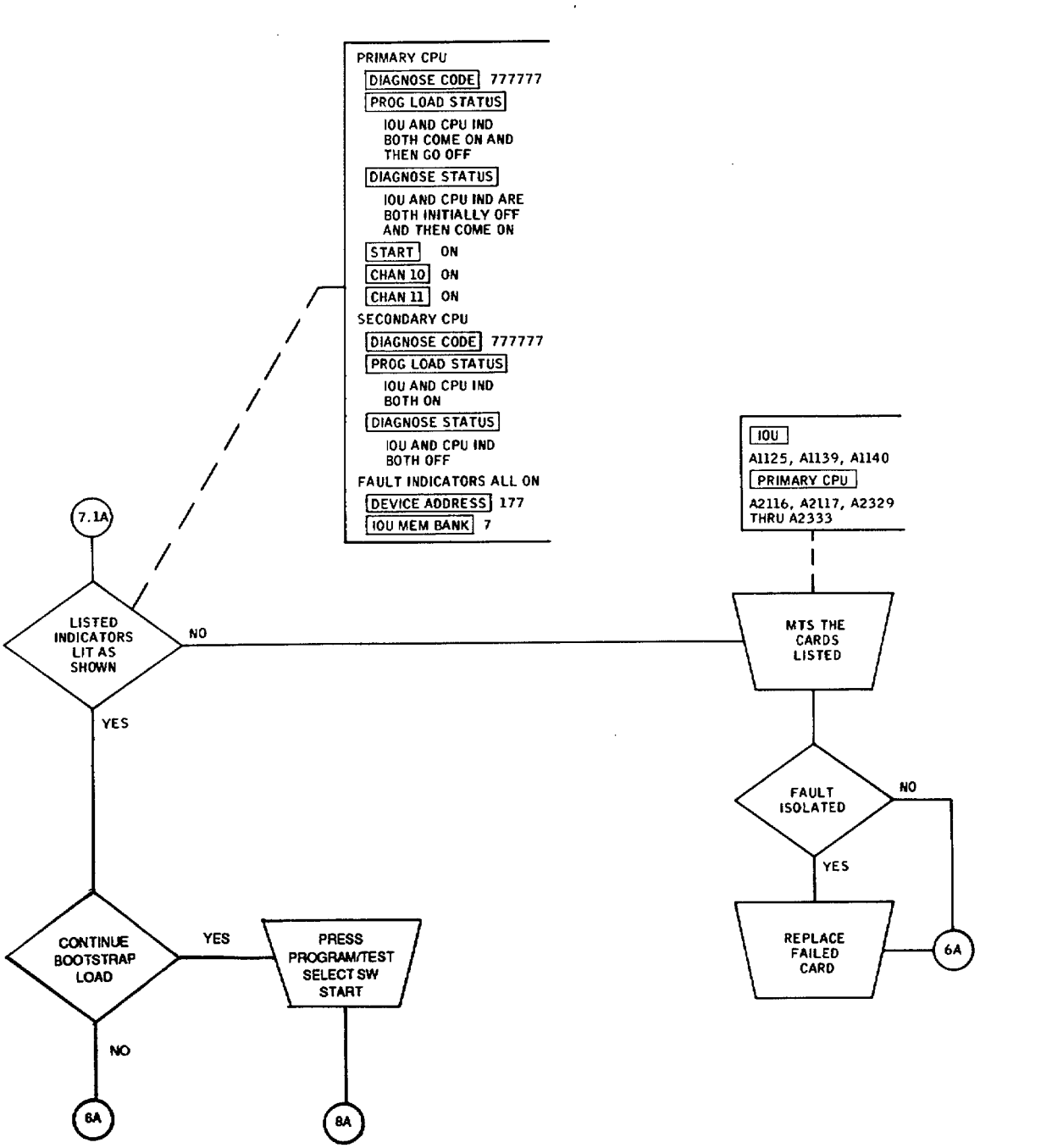


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 7 of 37)



MS012923

Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 7.1 of 37)

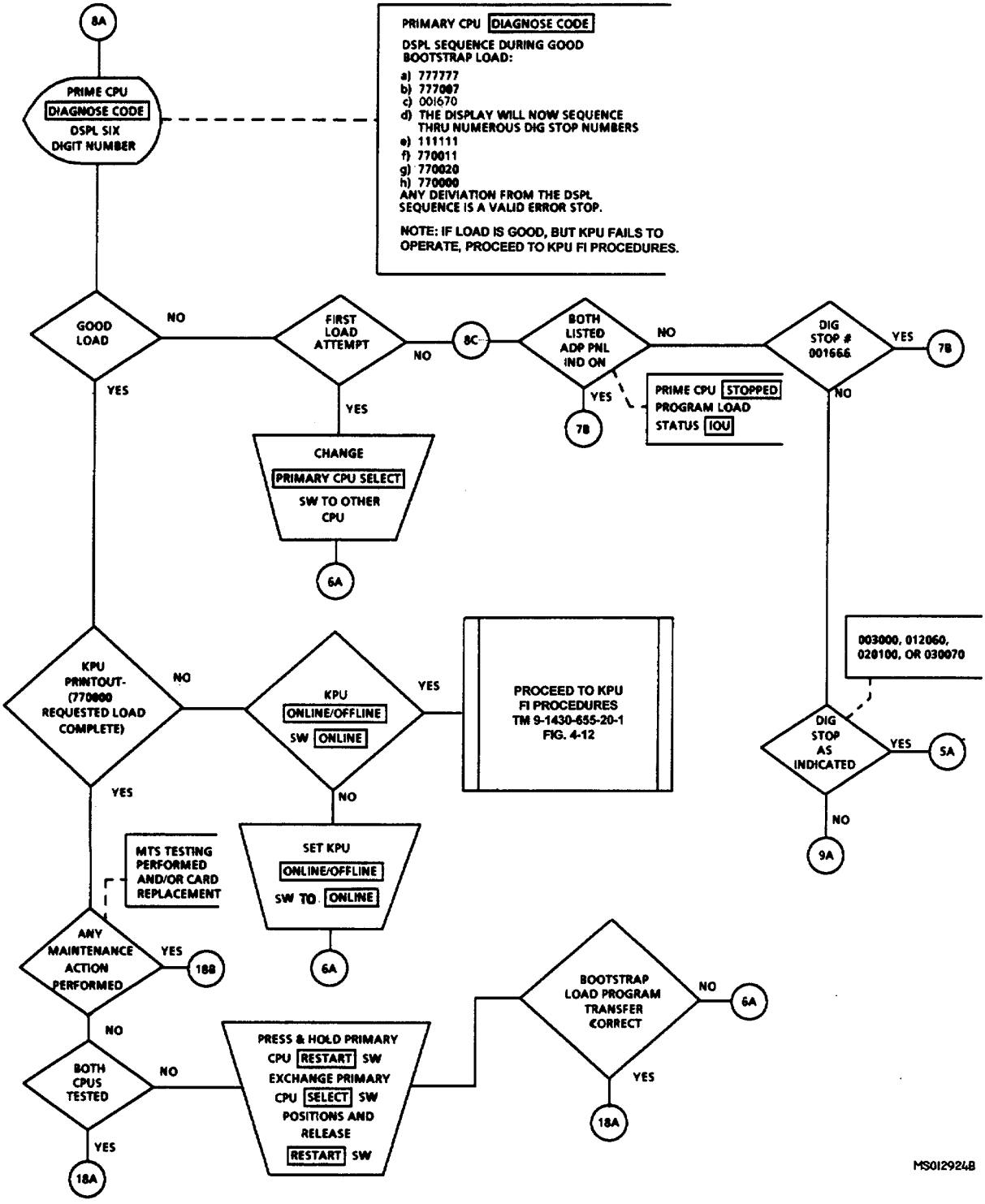


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 8 of 37)

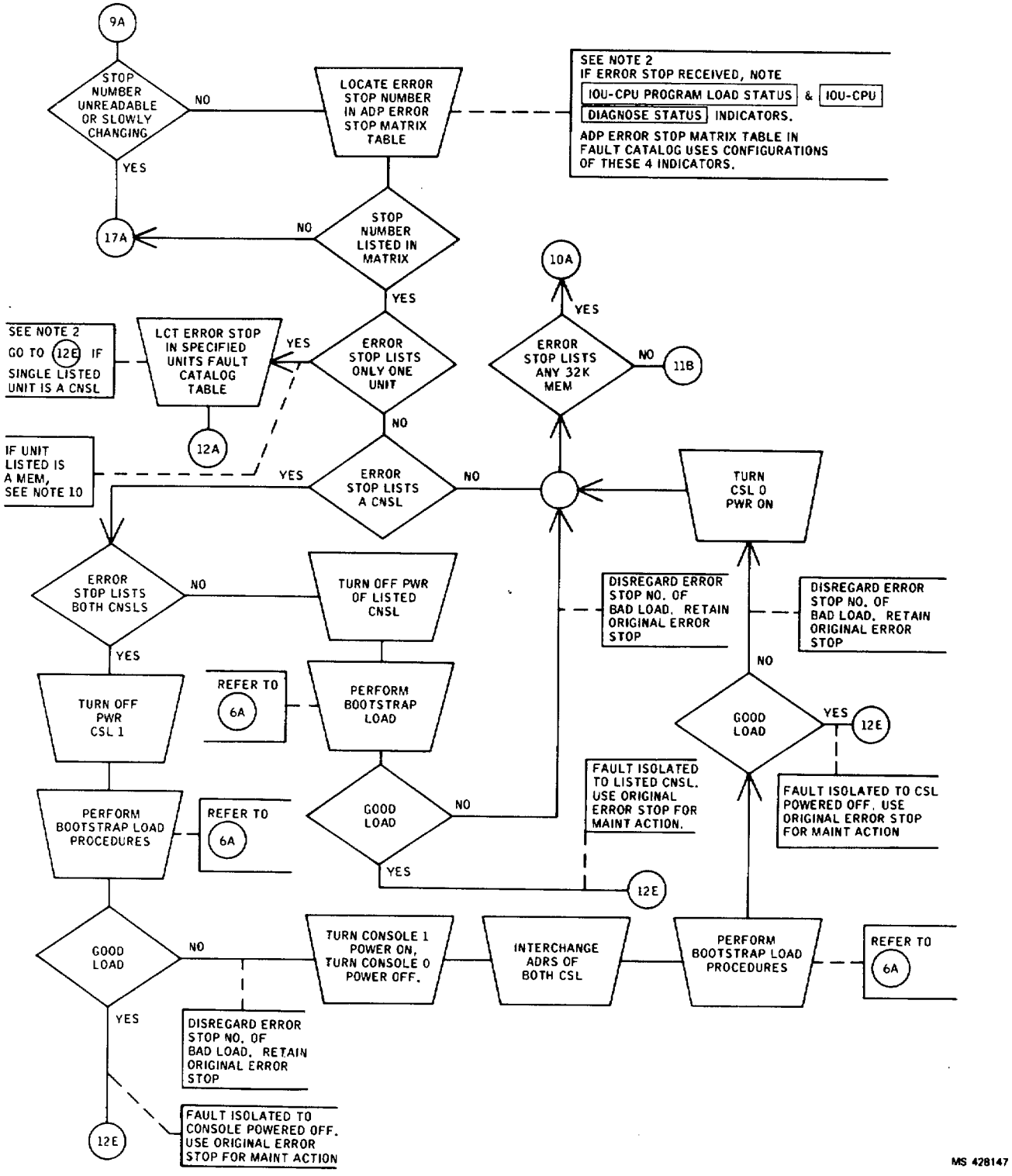
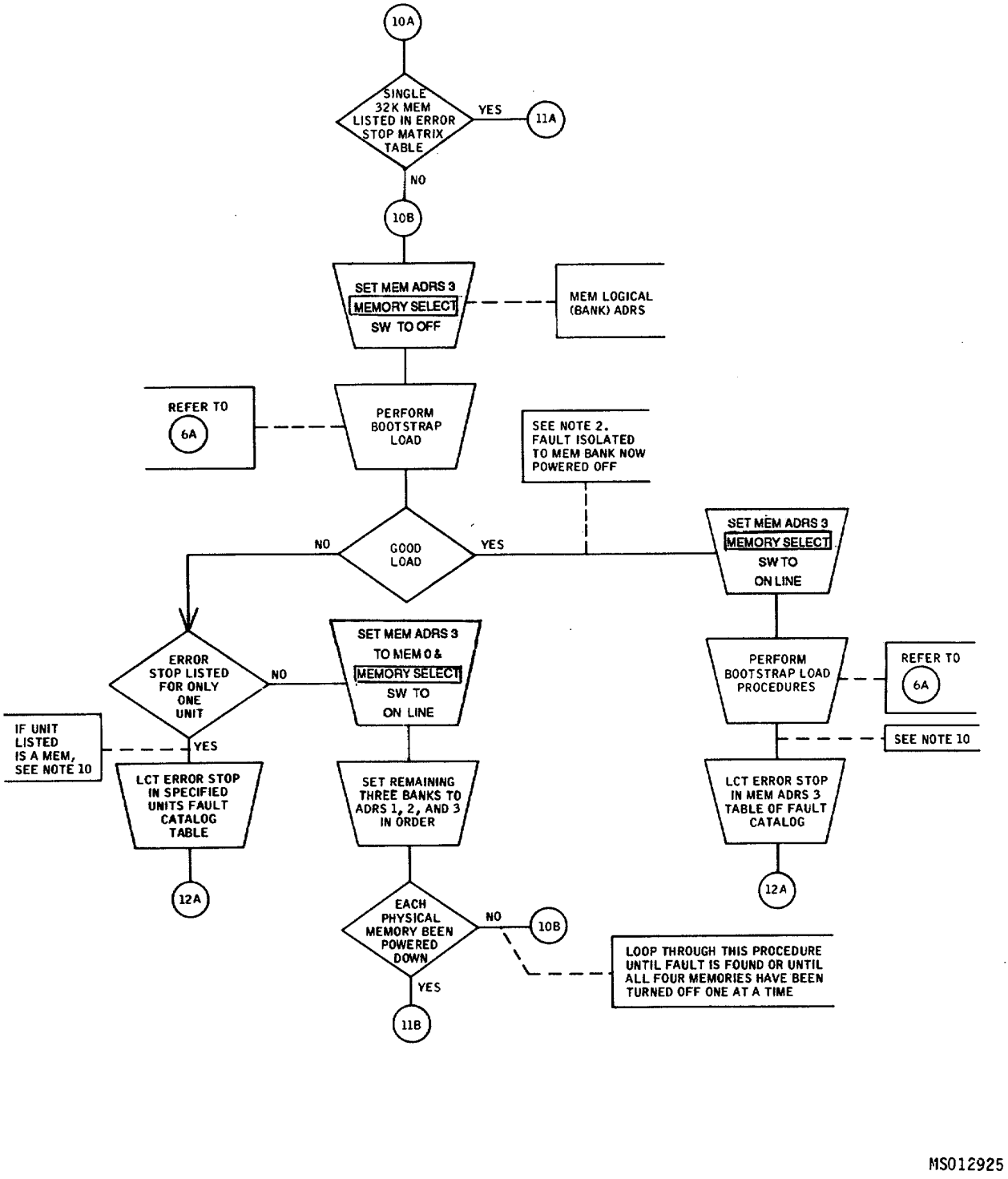


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 9 of 37)



MS012925

Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 10 of 37)

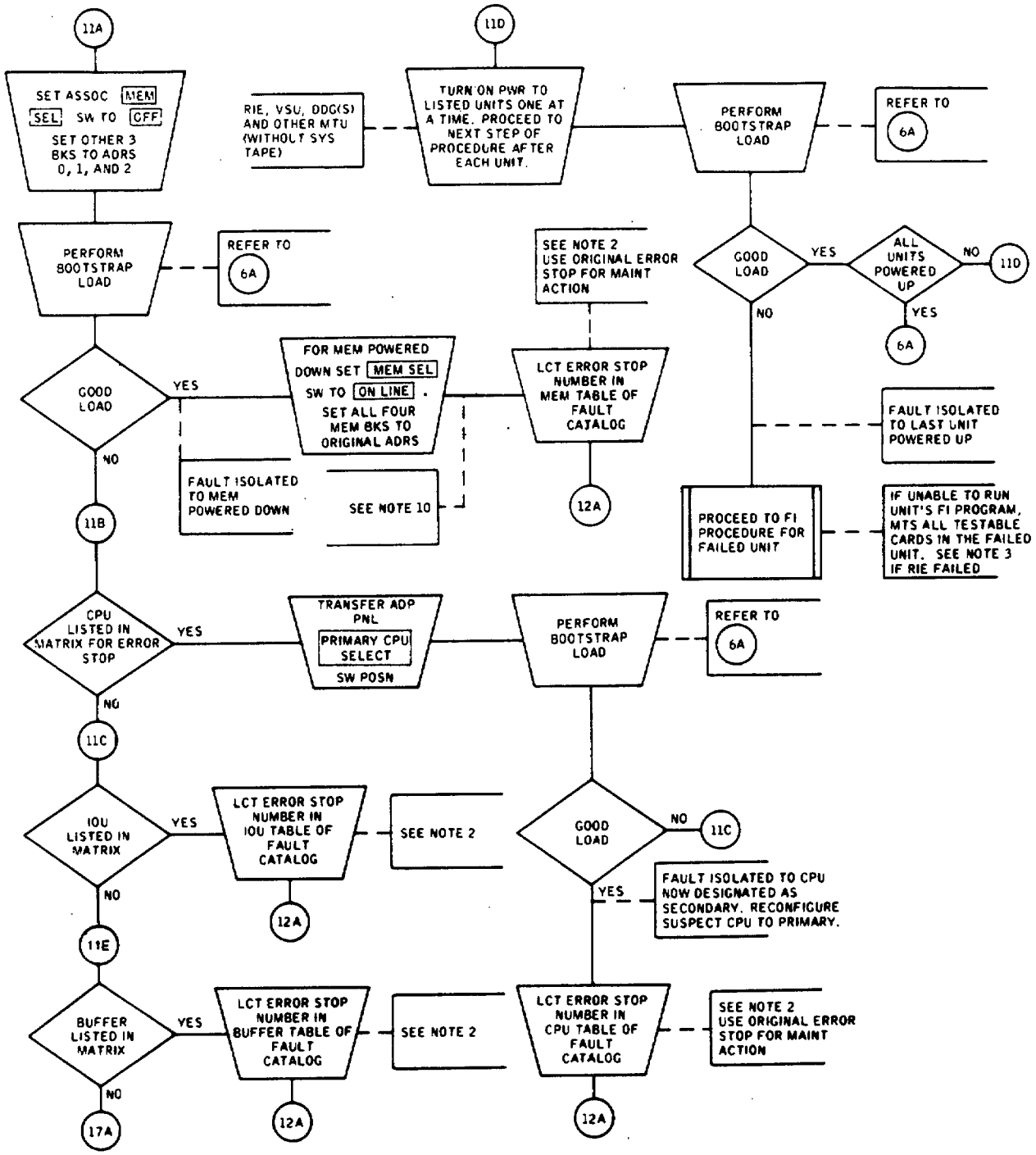


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 11 of 37)

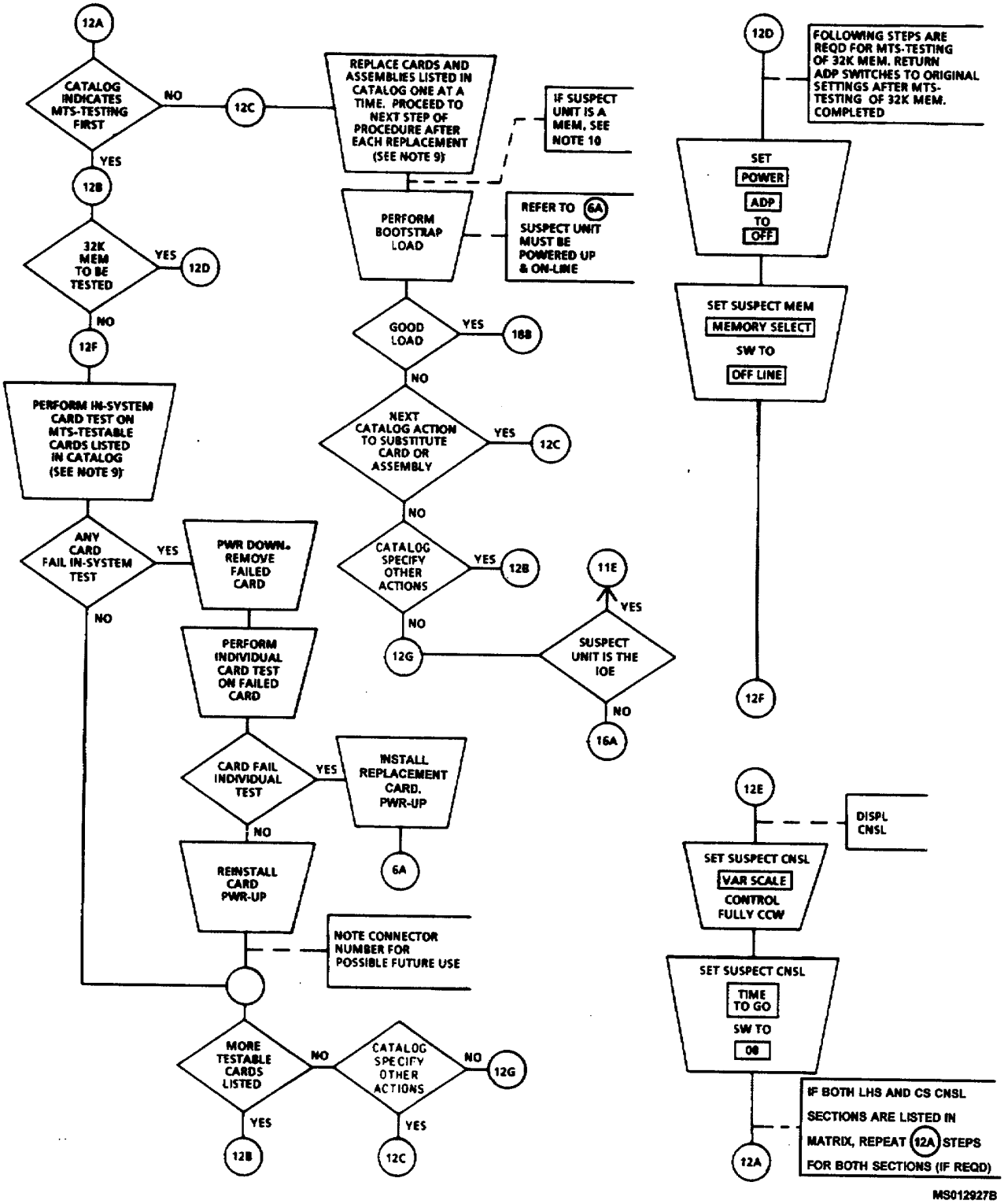
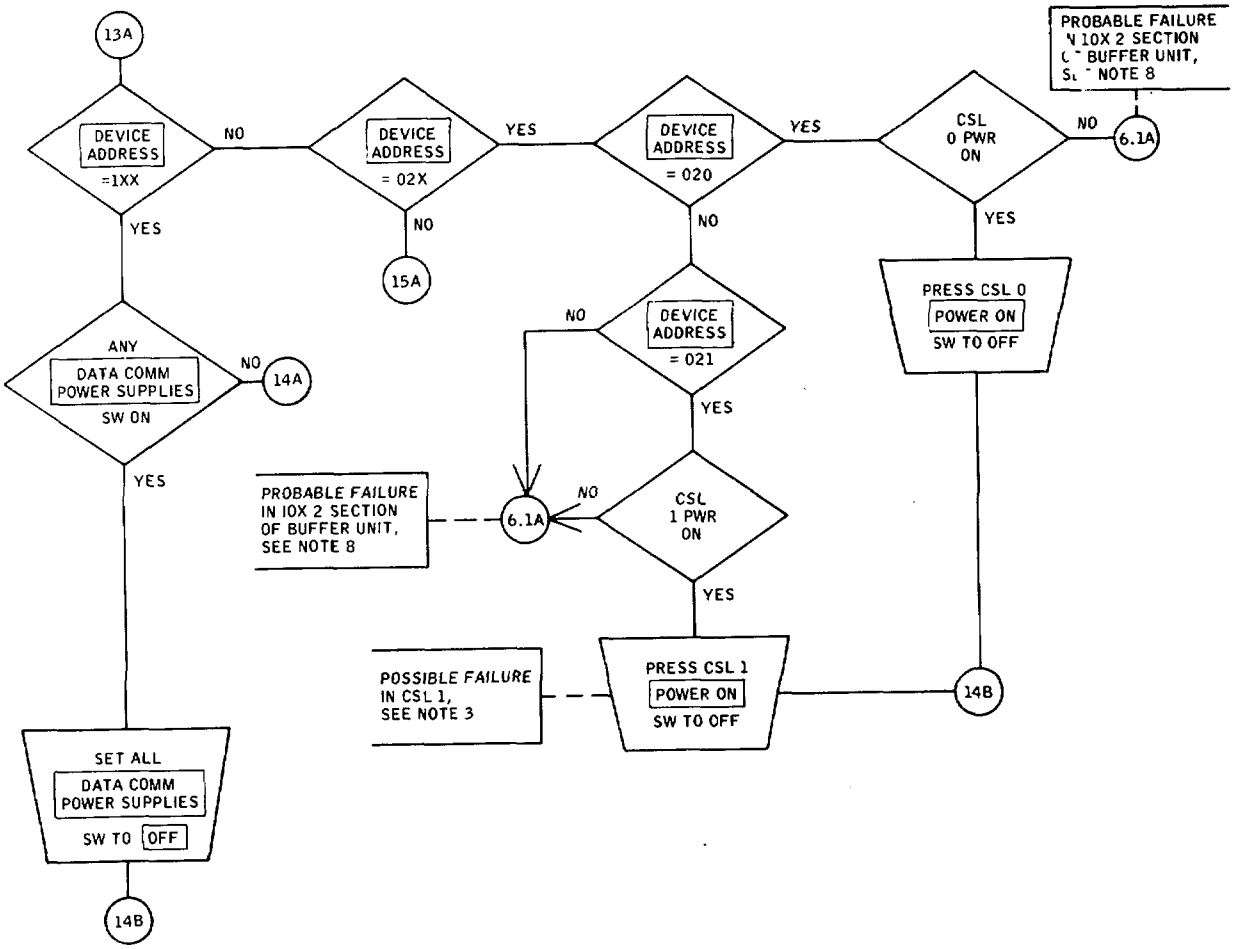


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 12 of 37)



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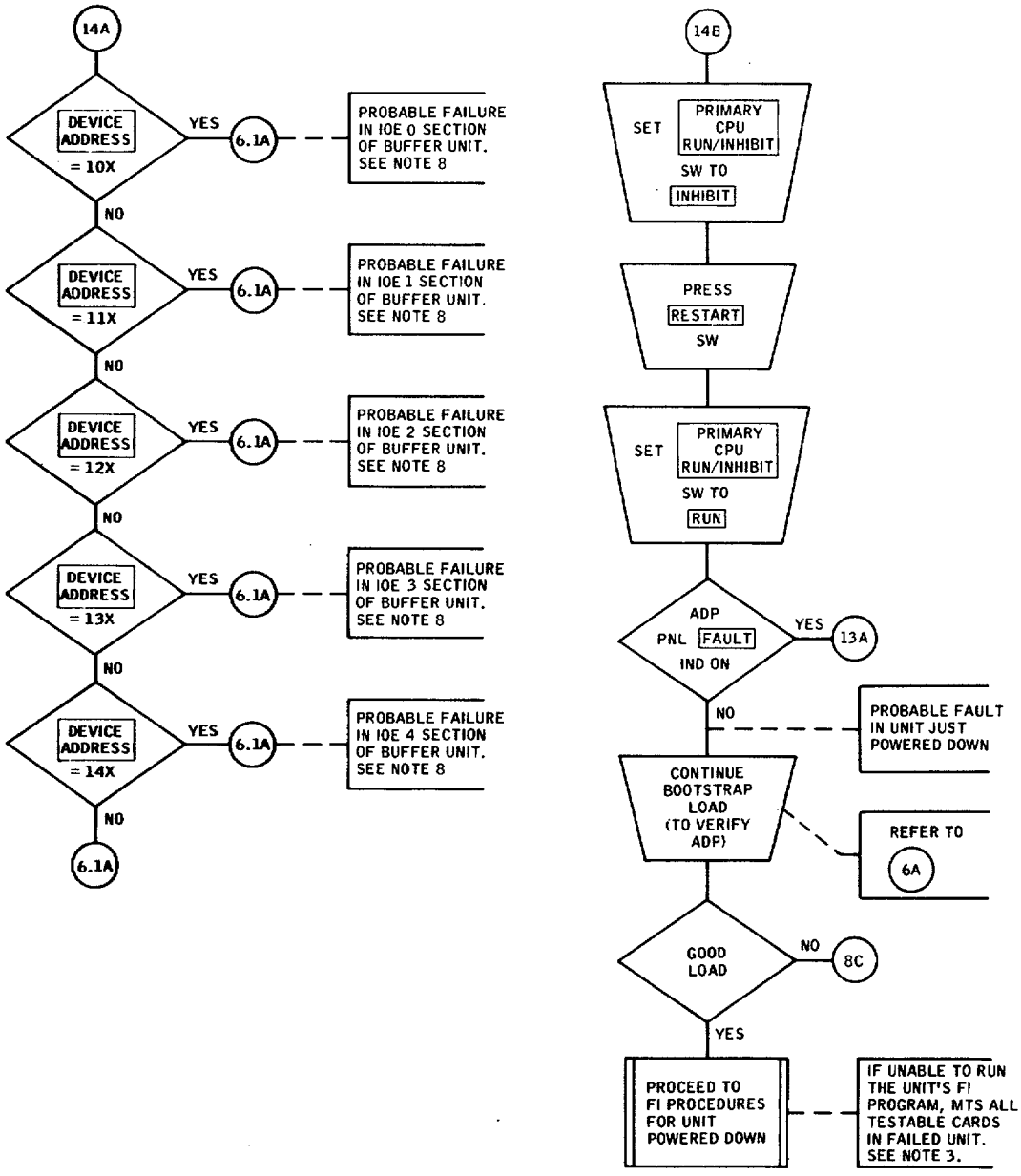
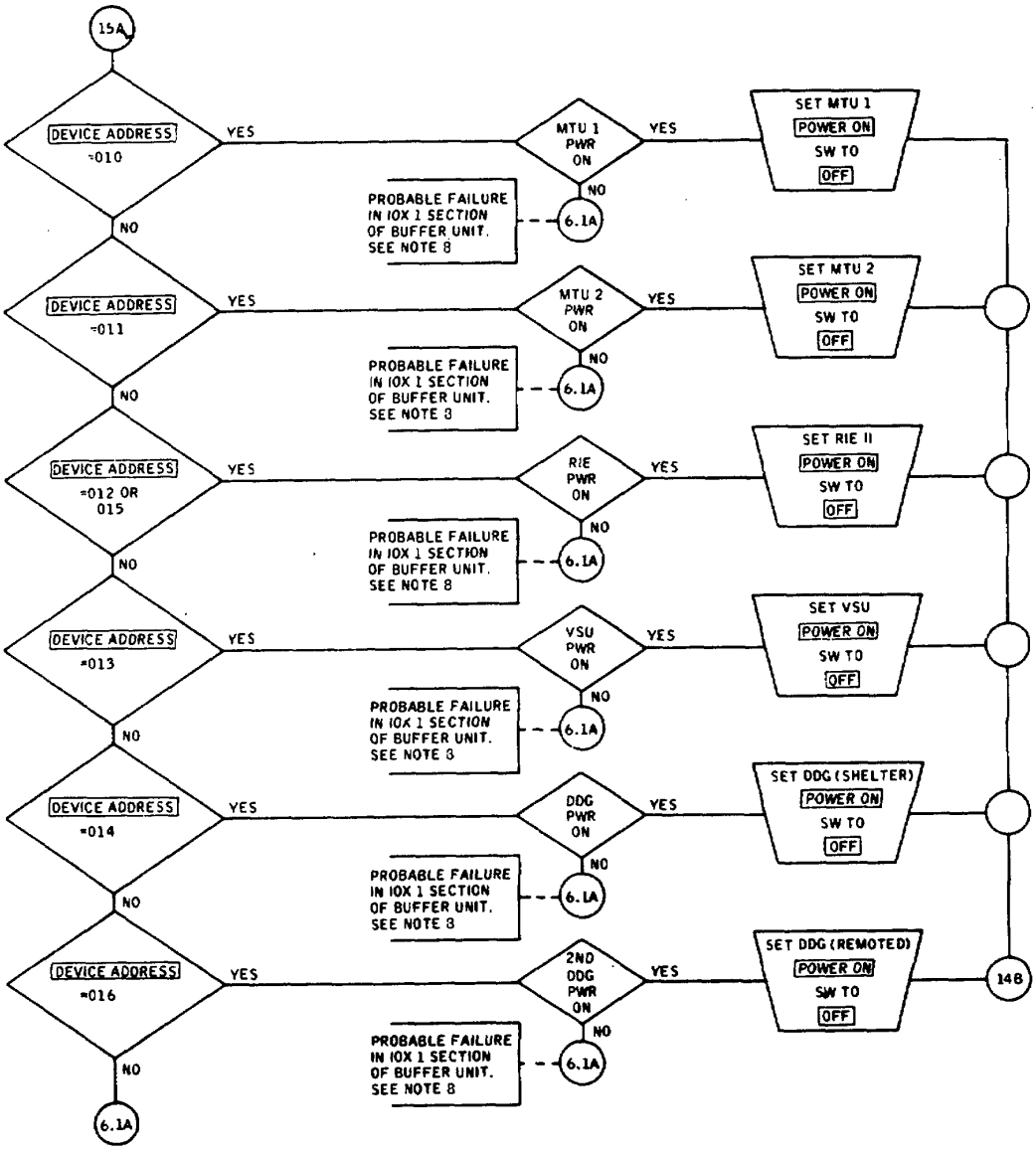
MS 428151

Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 13 of 37)



MS 428152

Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 14 of 37)



MS 428153

Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 15 of 37)

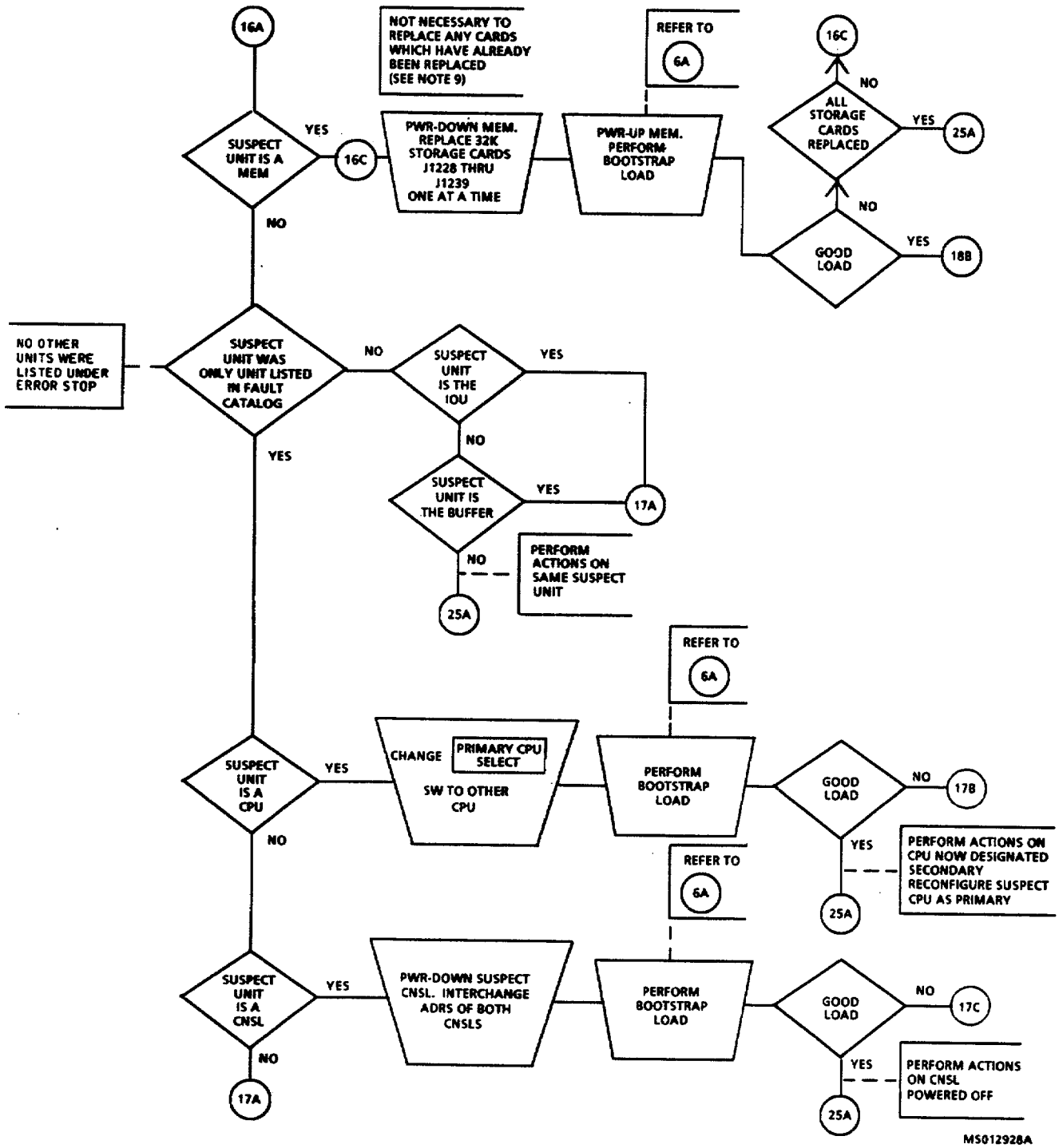


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 16 of 37)

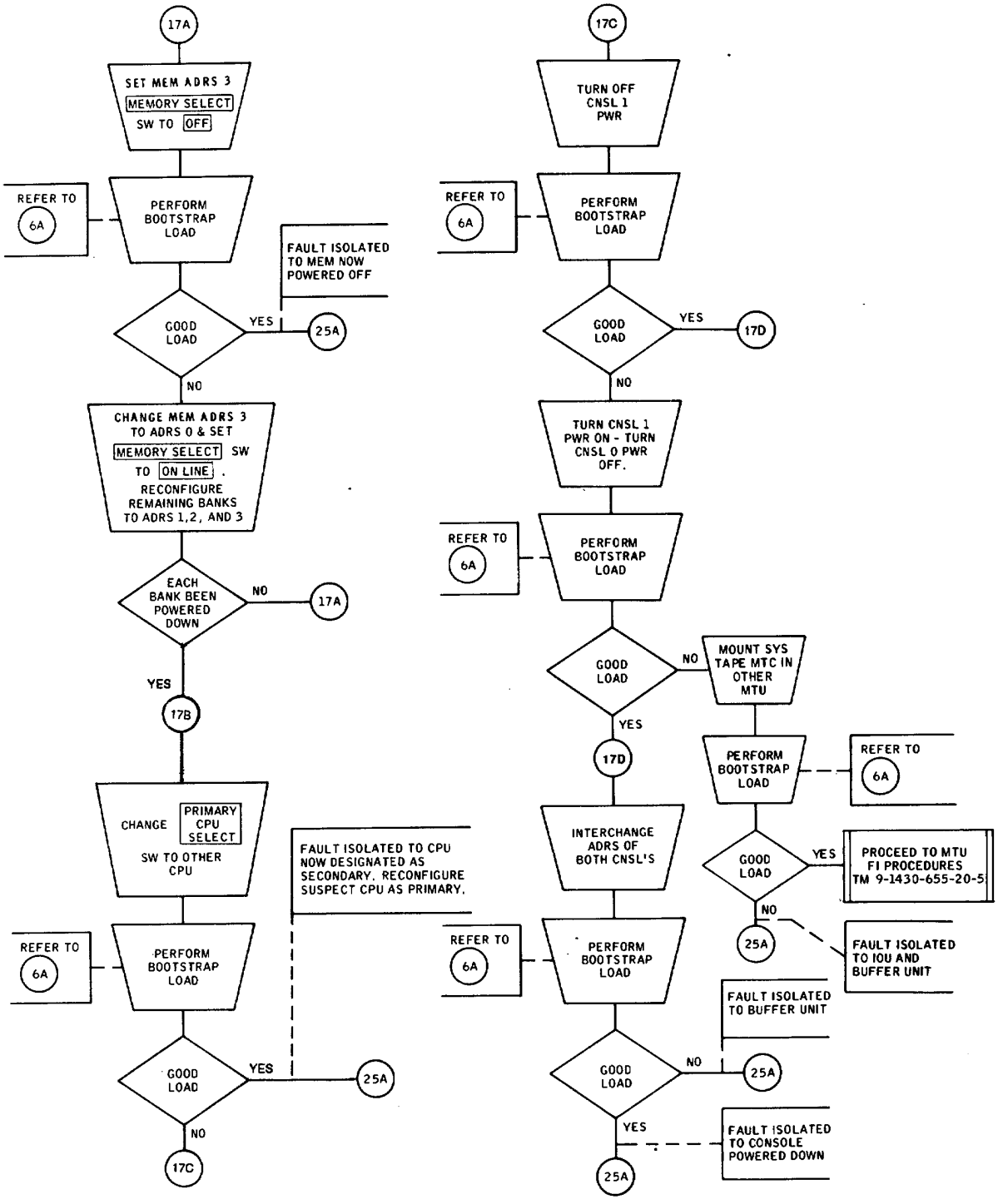


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 17 of 37)

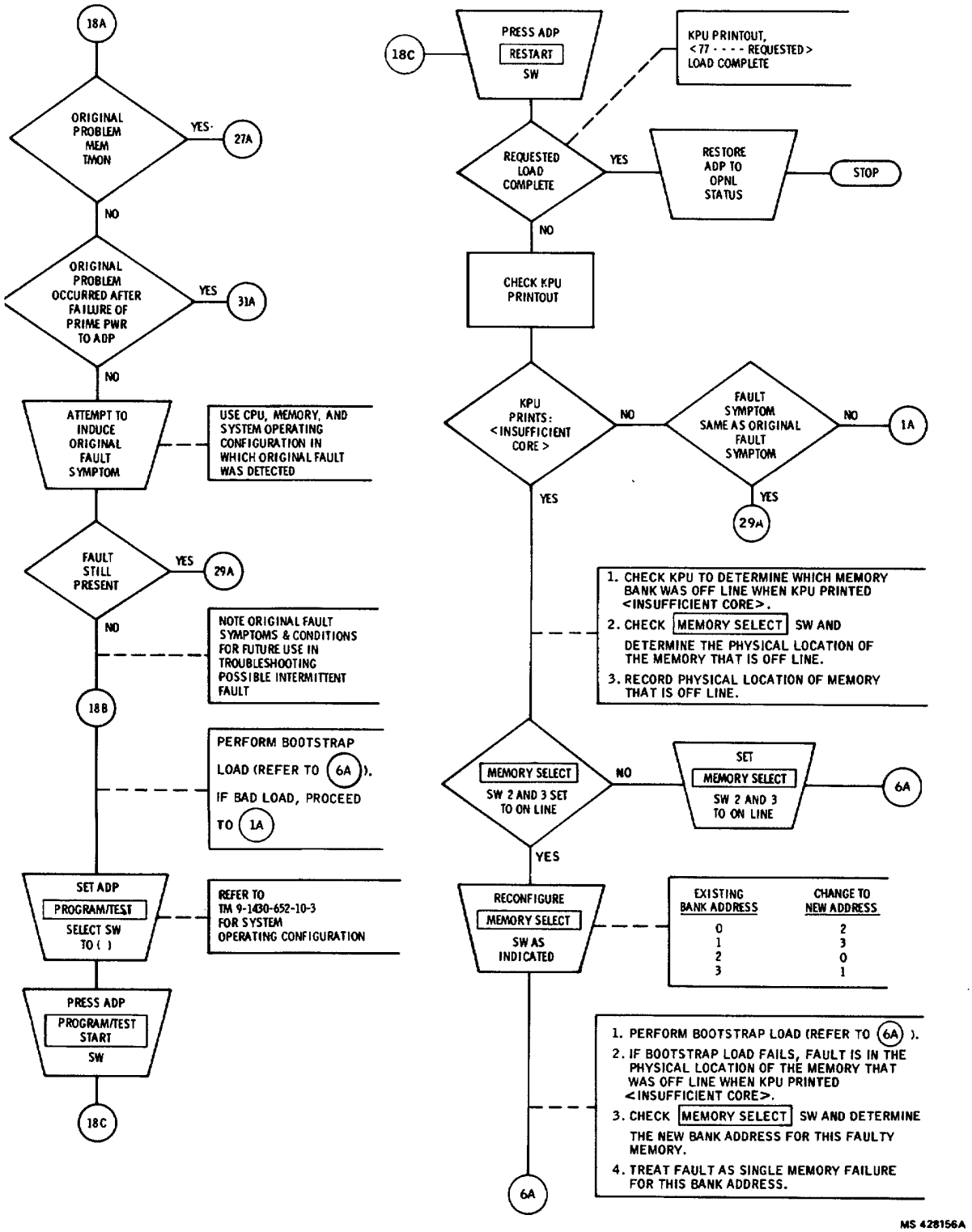
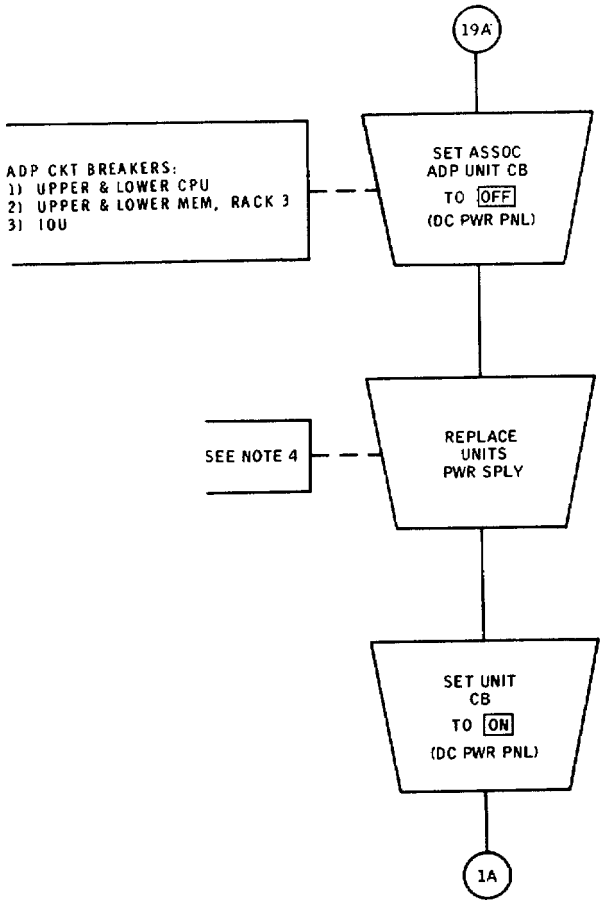
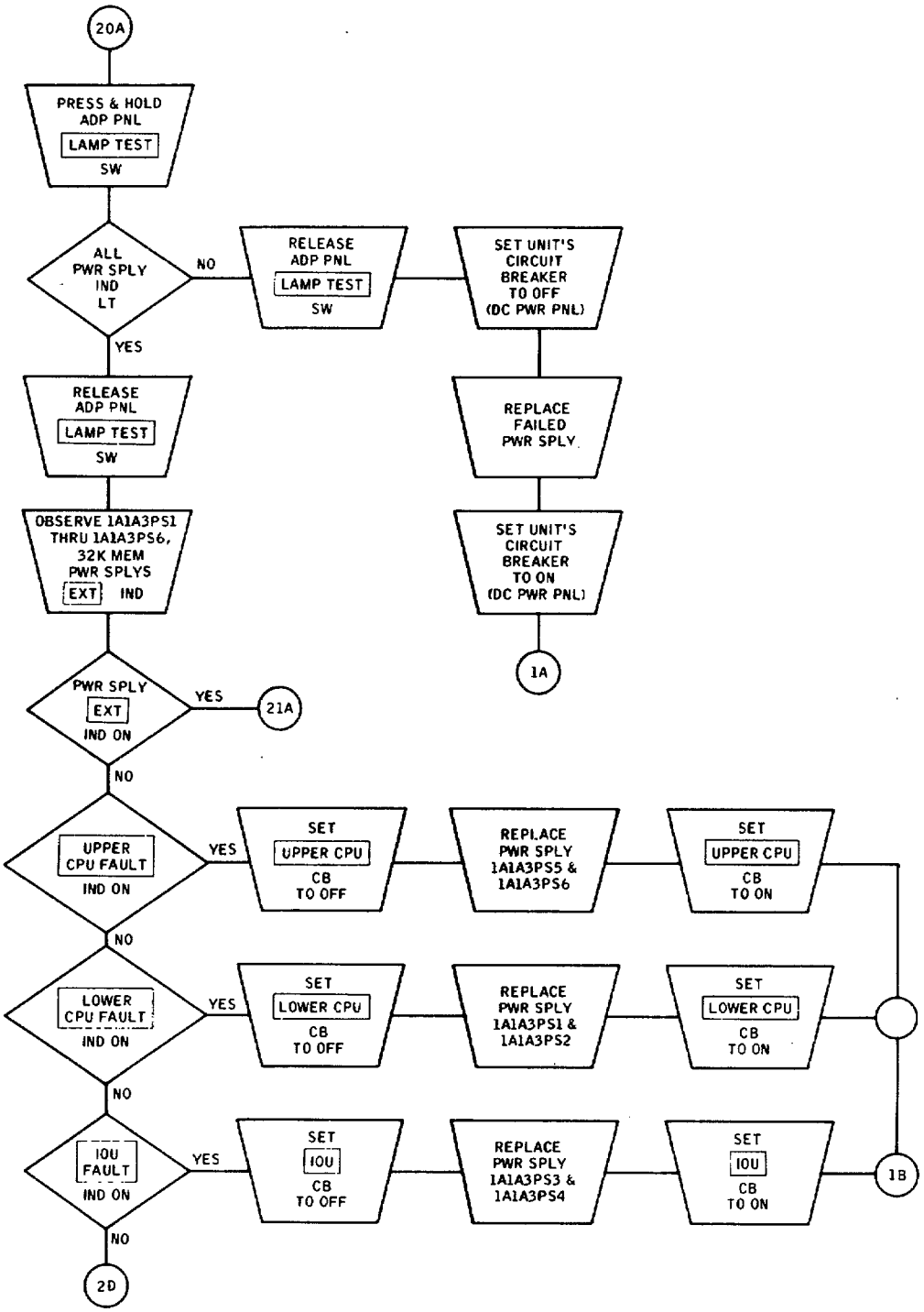


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 18 of 37)



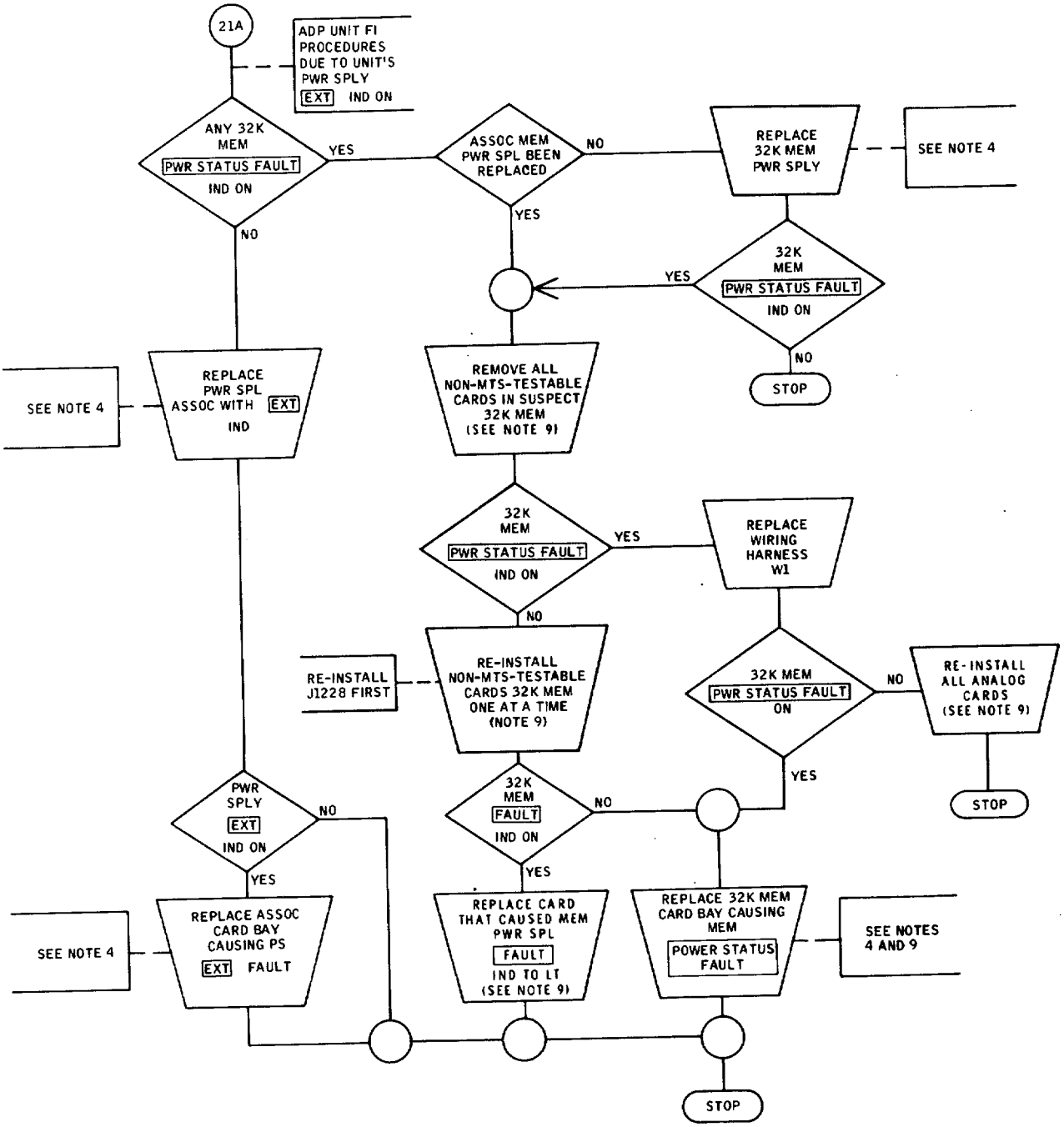
MS 428157

Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 19 of 37)



MS 428158

Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 20 of 37)



MS428159

Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 21 of 37)

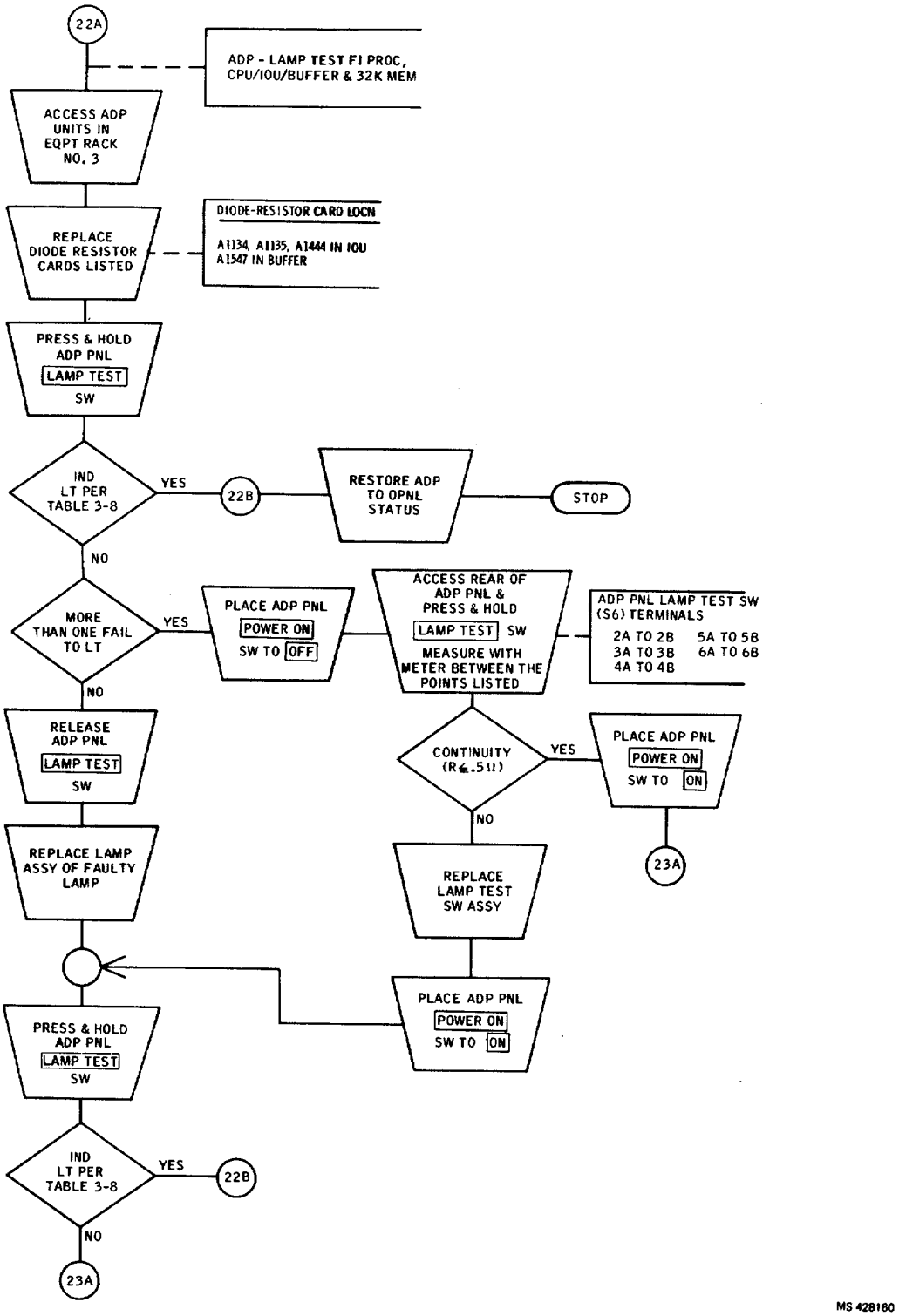


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 22 of 37)

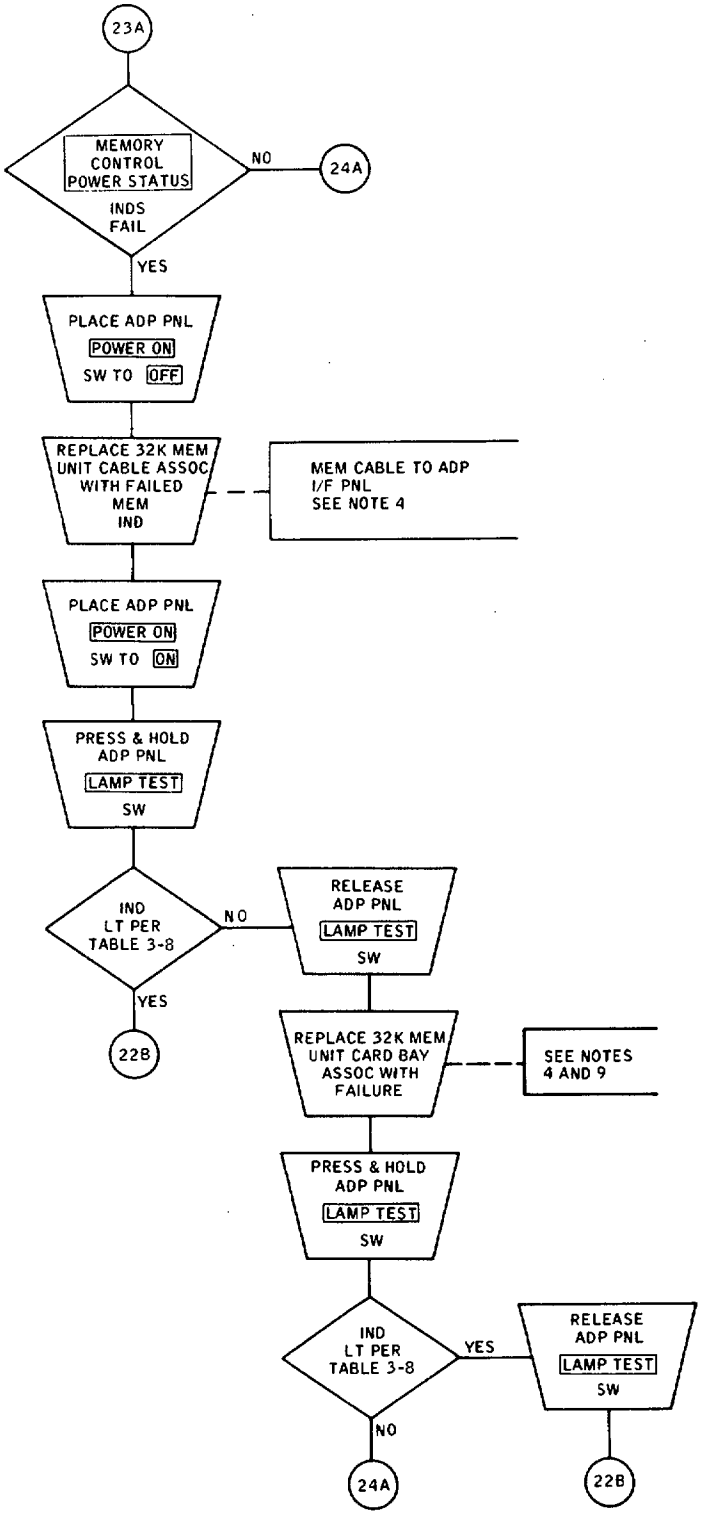


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 23 of 37)

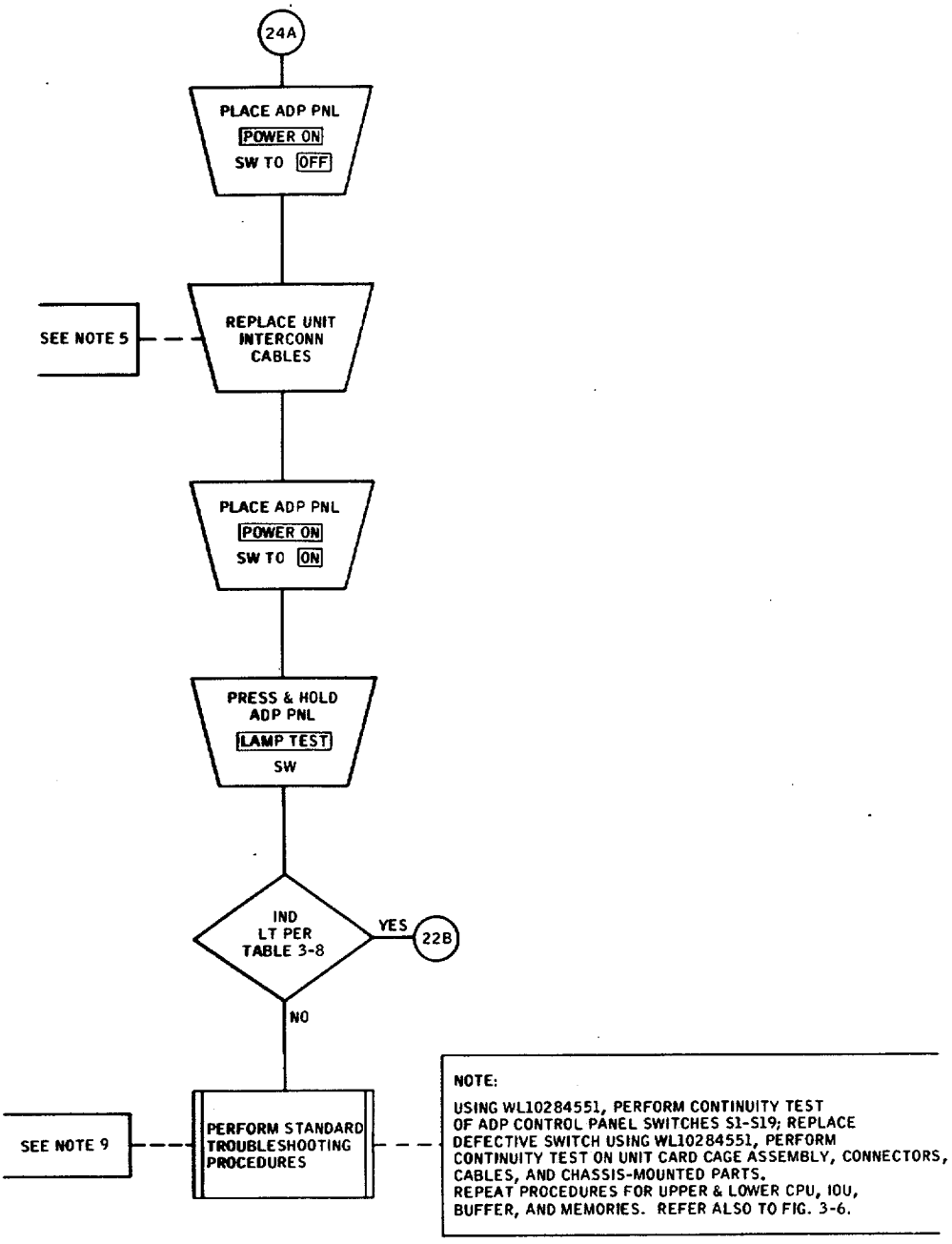


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 24 of 37)

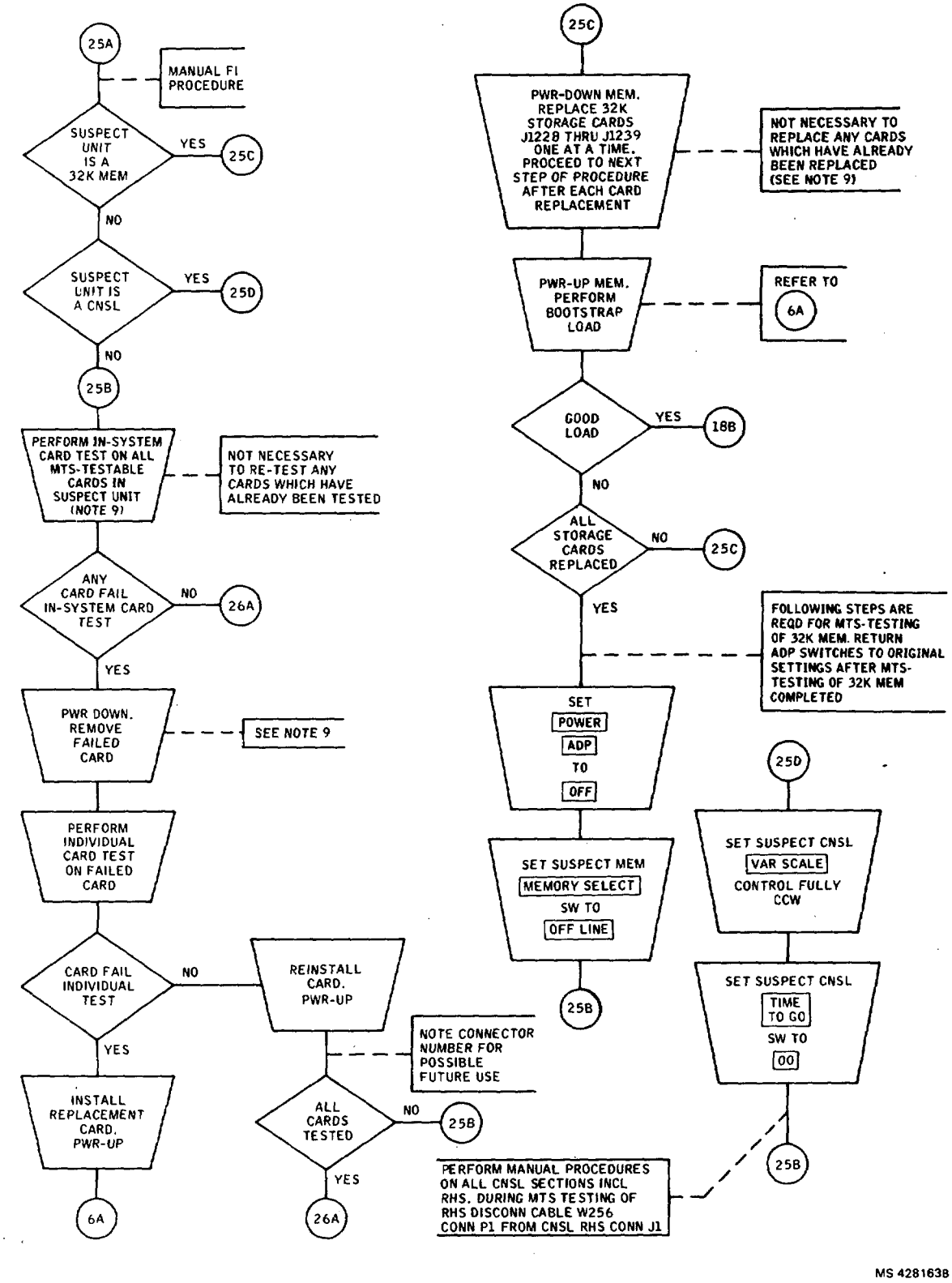


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 25 of 37)

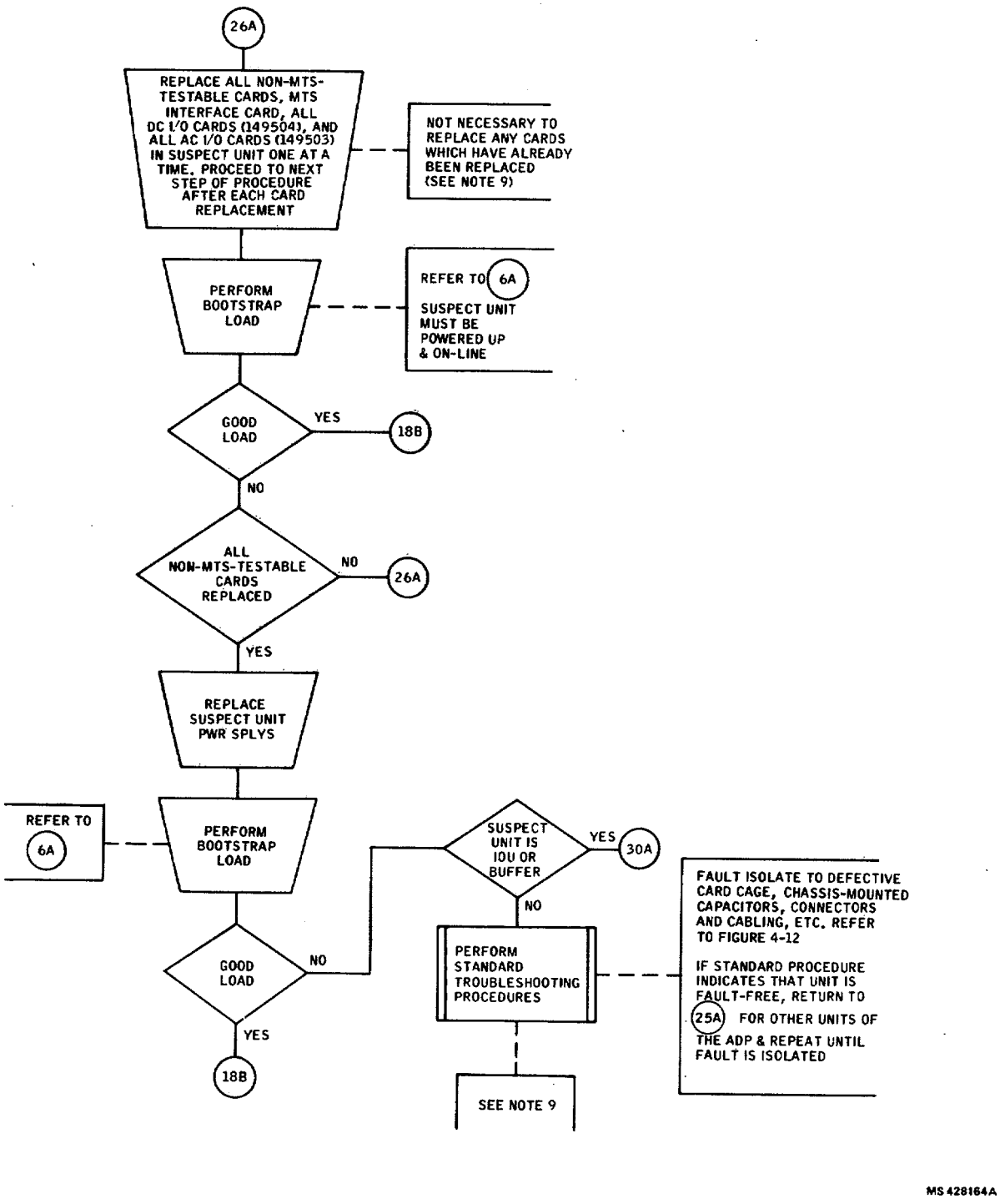


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 26 of 37)

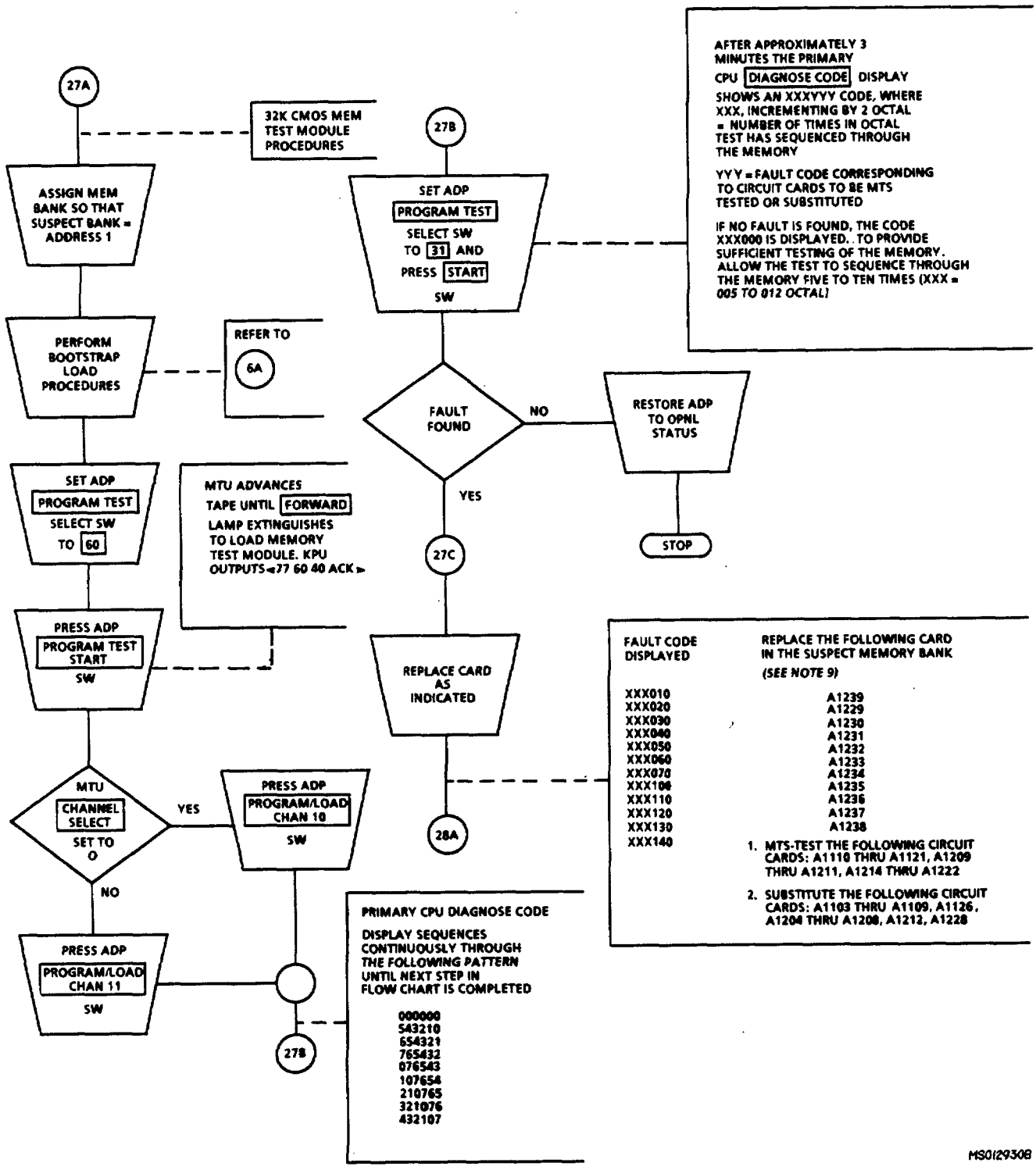


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 27 of 37)

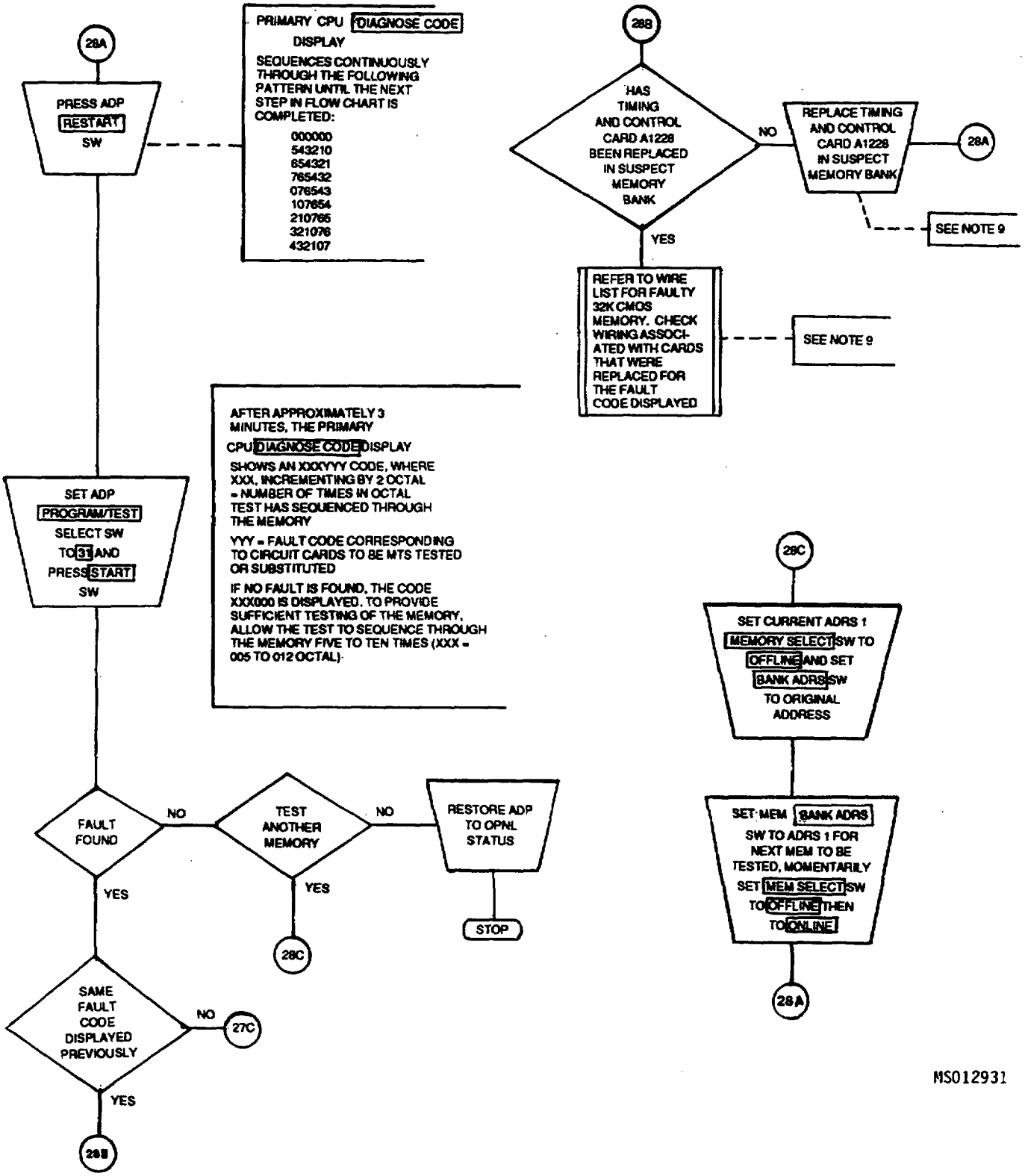


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 28 of 37)

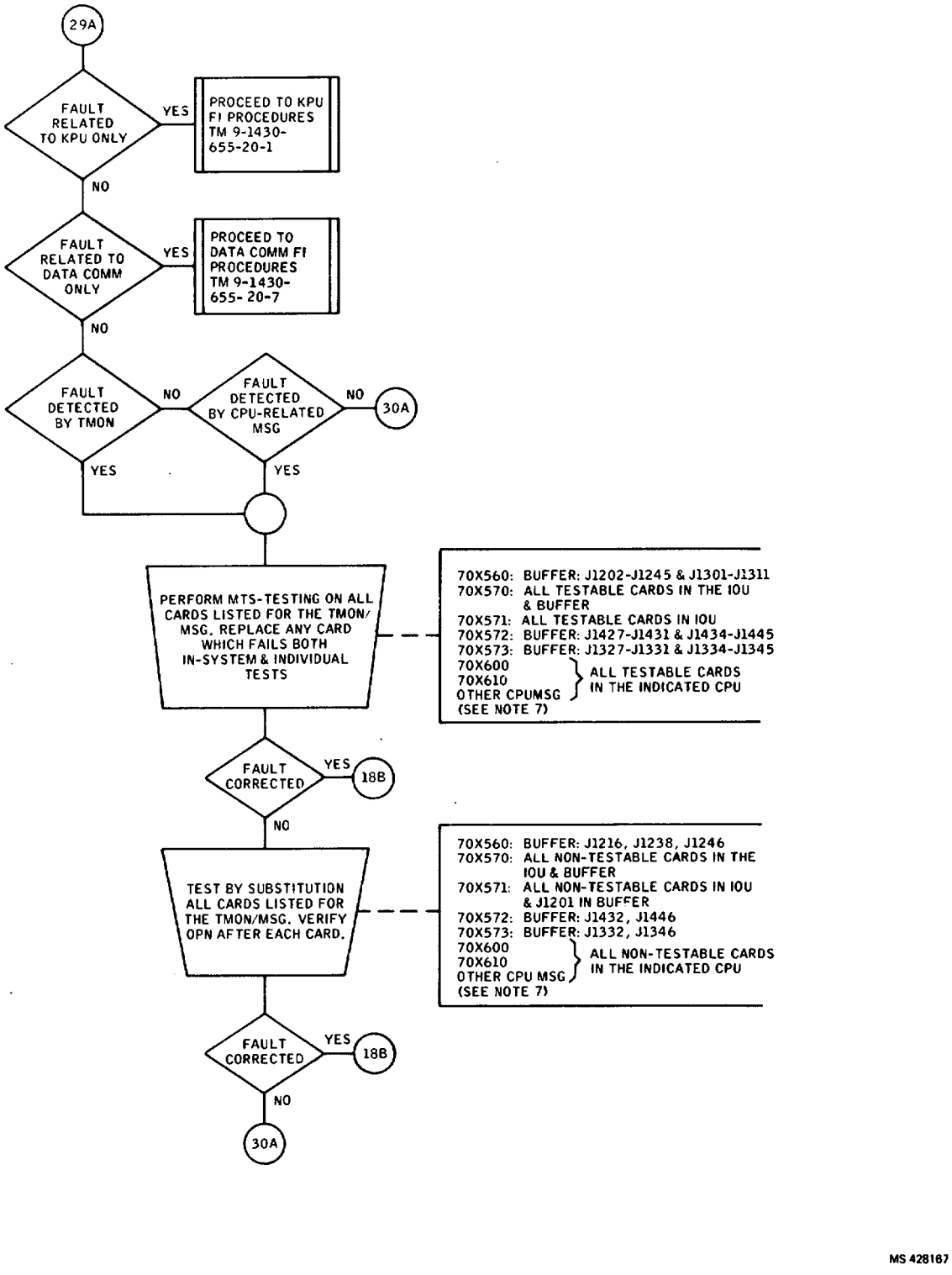


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 29 of 37)

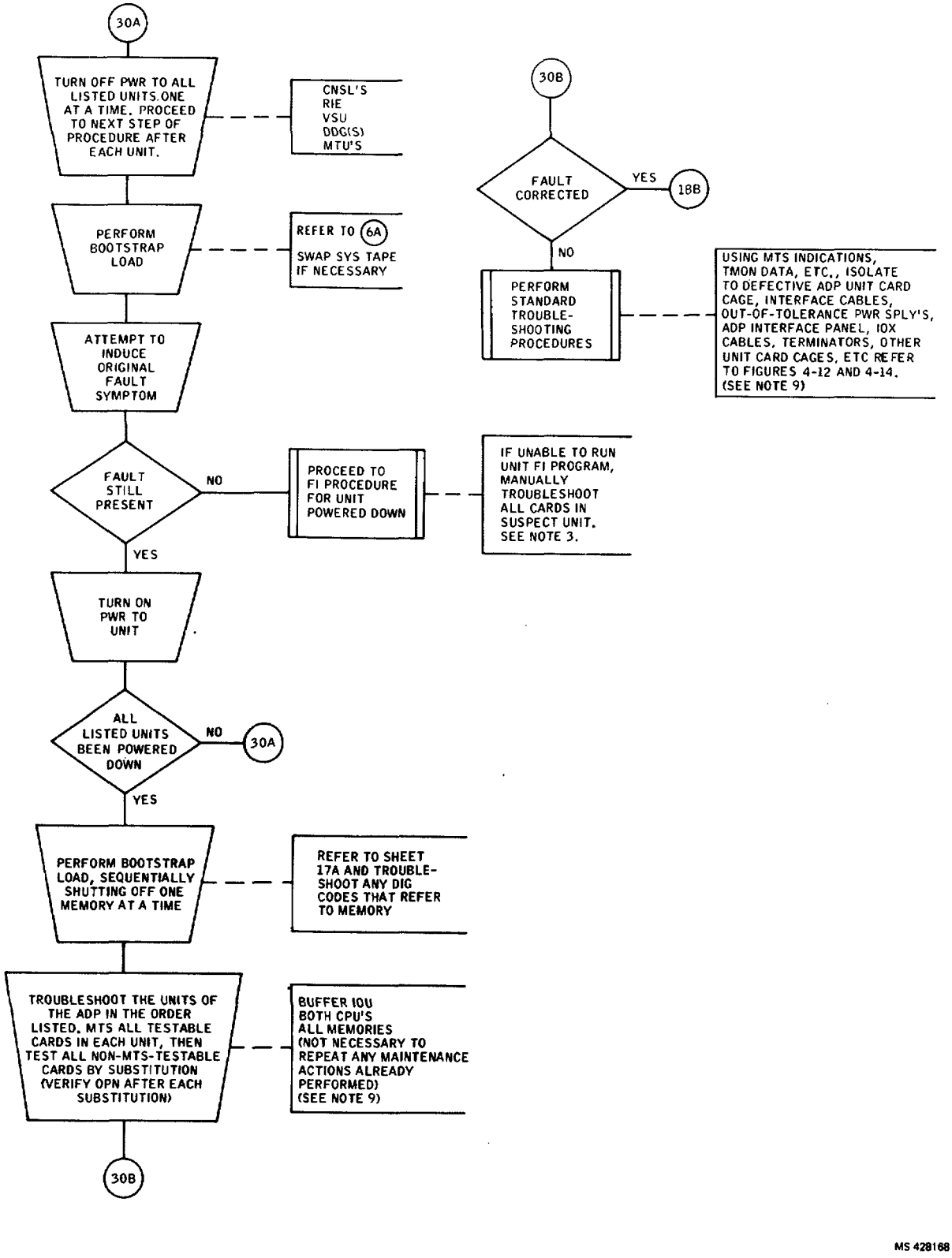


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 30 of 37)

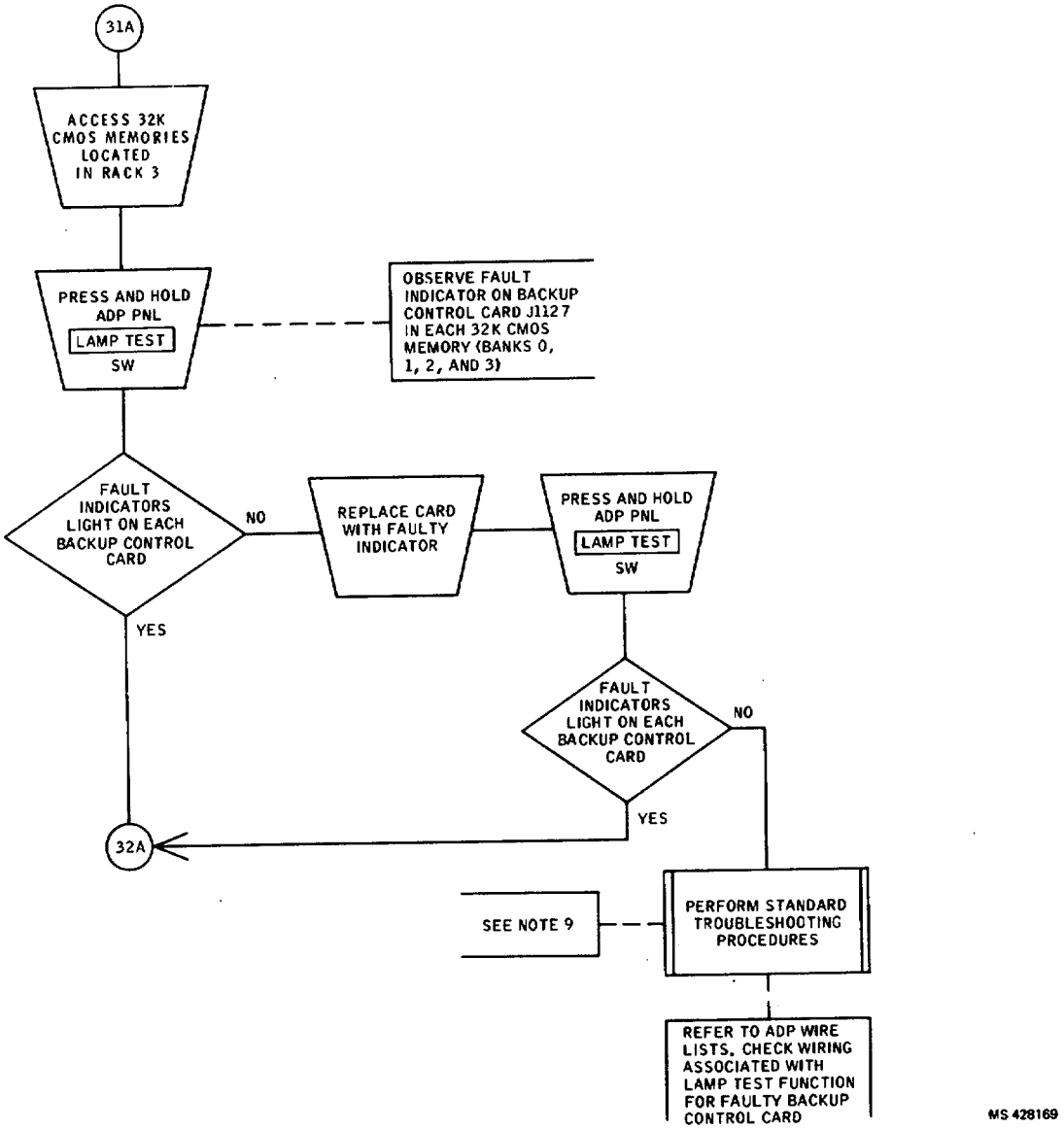


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 31 of 37)

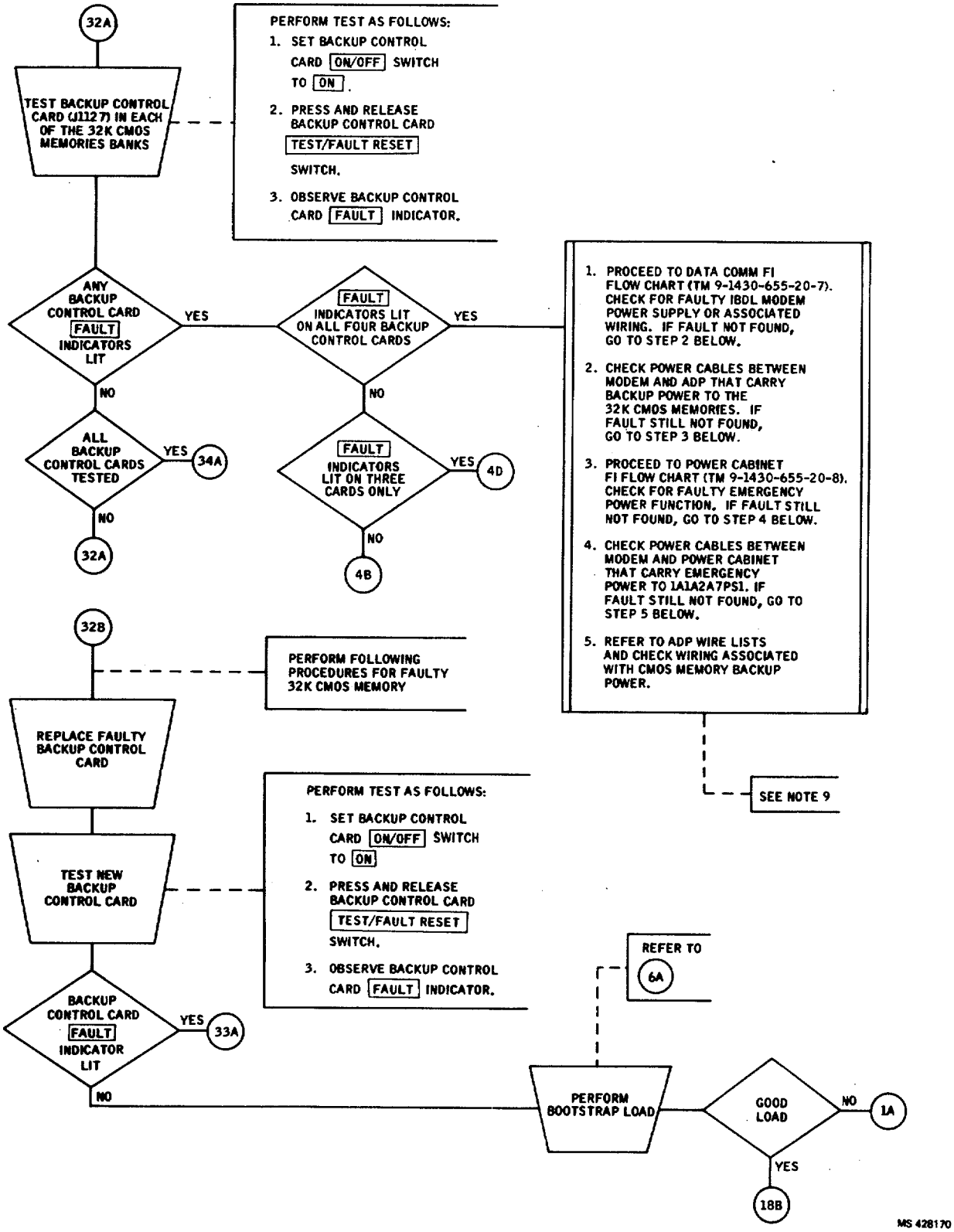


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 32 of 37)

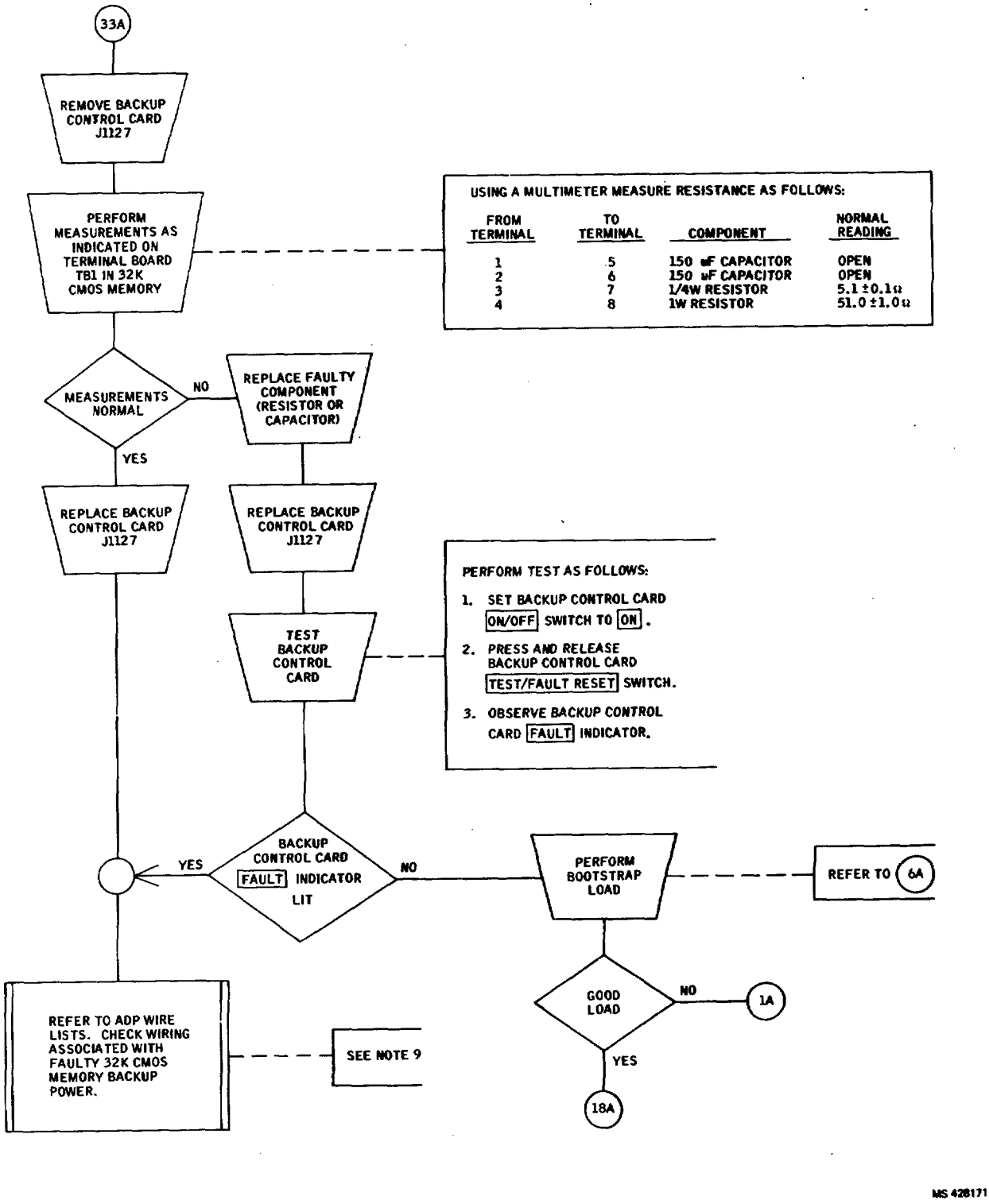


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 33 of 37)

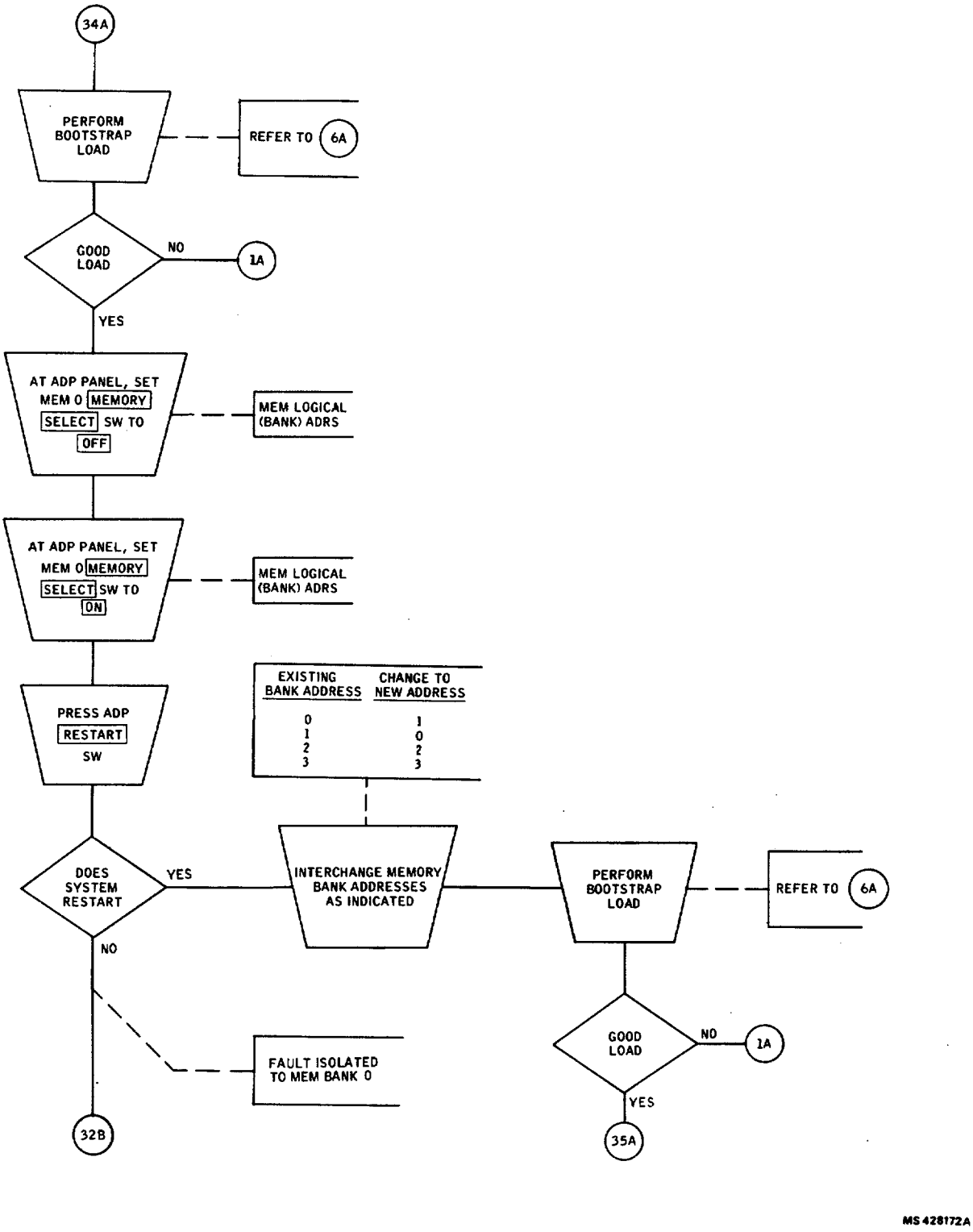


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 34 of 37)

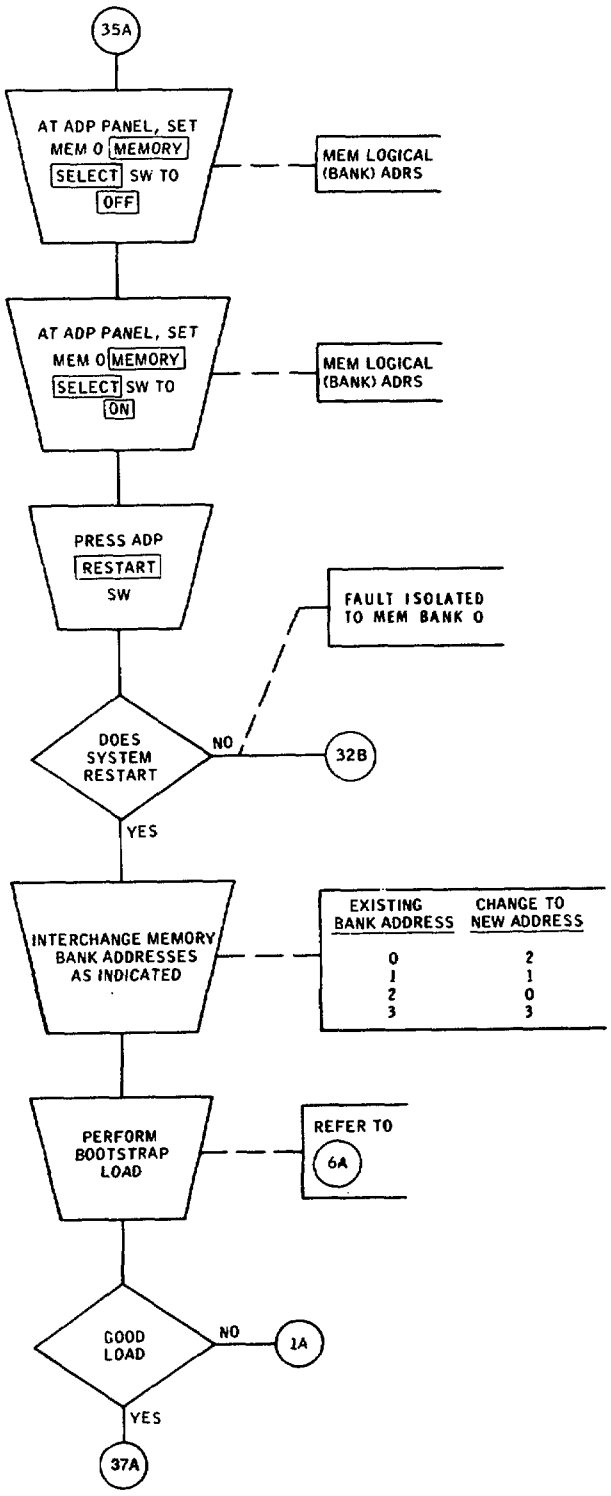


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 35 of 37)

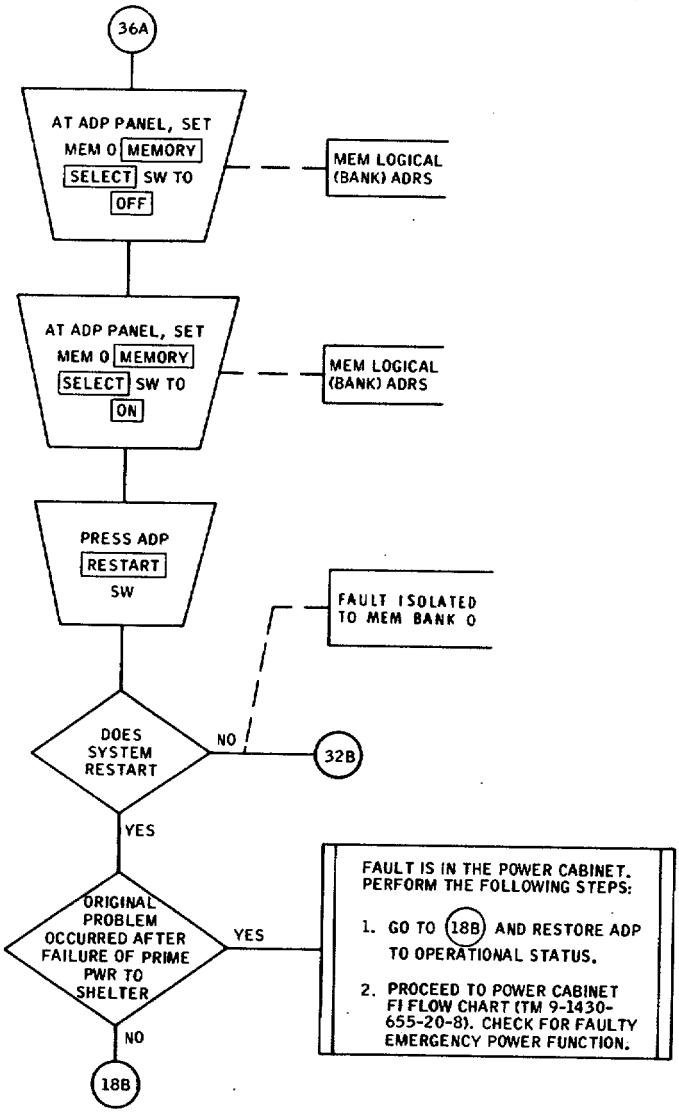


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 36 of 37)

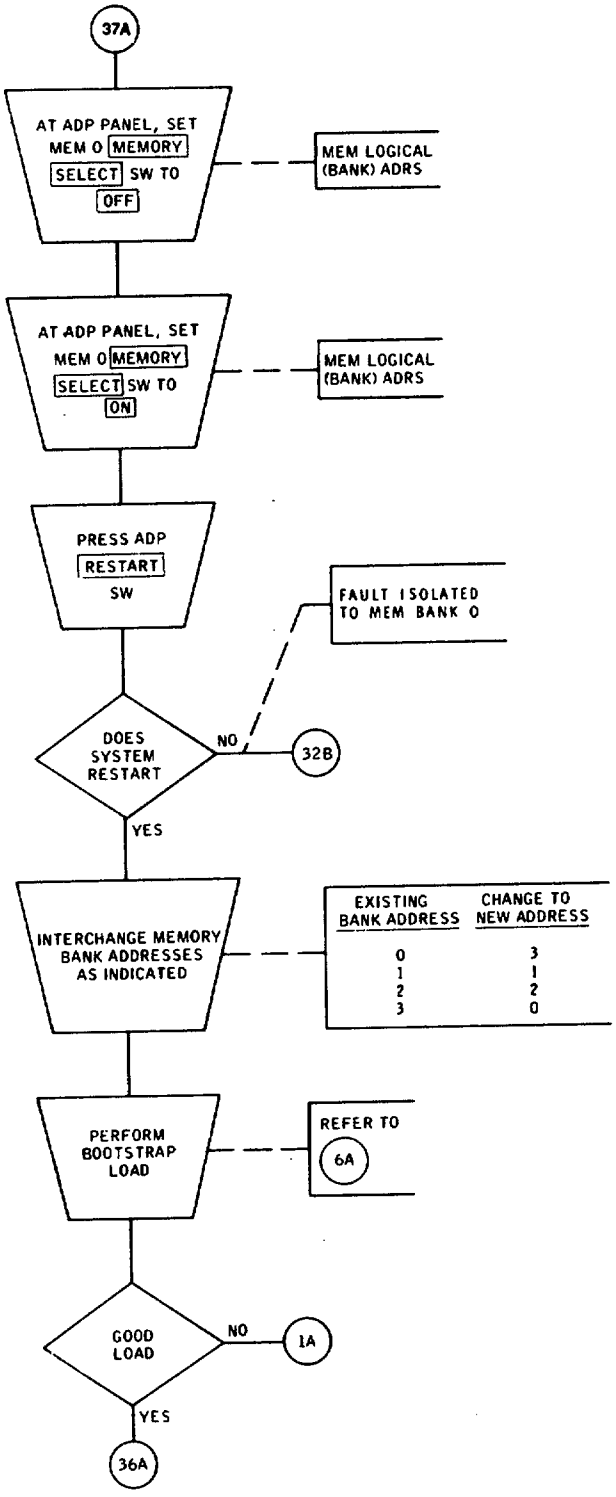


Figure 3-13. ADP Fault Isolation Flow Chart (Sheet 37 of 37)

Table 3-8. ADP Lamp Test Indications

Indicator	Indication
NOTE Due to noise in lamp test circuit, one or more LED readouts can be distorted. This does not negate the test and is considered normal.	
ADP STATUS AND CONTROL	
POWER	
UPPER CPU ON/FAULT	On
LOWER CPU ON/FAULT	On
IOU ON/FAULT	On
ADP STATUS	
UPPER CPU	
DIAGNOSE STATUS IOU/CPU	On
DIAGNOSE CODE	777777
PROG LOAD STATUS IOU/CPU	On
LOWER CPU	
DIAGNOSE STATUS IOU/CPU	On
DIAGNOSE CODE	777777
PROG LOAD STATUS IOU/CPU	On
PRIMARY CPU	
STOPPED	On
RESTART	Off
PROGRAM LOAD	
CHAN 10	On
CHAN 11	On
PROGRAM/TEST	
START	On
FAULT	
PRIME CPU	On
SEC CPU	On
IOU	On
TIME OUT IOU/PROG	On
DEVICE ERROR PARITY/T-OUT	On
MEMORY ERROR	
PARITY IOU/CPU	On
TIME OUT IOU/CPU	On
DEVICE ADDRESS	177
IOU MEM BANK	7

Table 3-8. ADP Lamp Test Indications
-Continued

Indicator	Indication
SECONDARY CPU	
STOPPED	On
RESTART	Off
START	On
DISPLAY OUTPUT UNIT	
RESTART	Off
MEMORY CONTROL	
POWER STATUS	
MEMORY 1 ON/FAULT	On
MEMORY 2 ON/FAULT	On
MEMORY 3 ON/FAULT	On
MEMORY 4 ON/FAULT	On
MEMORY 5 ON/FAULT	Not functional
MEMORY 6 ON/FAULT	Not functional
MEMORY 7 ON/FAULT	Not functional
MEMORY 8 ON/FAULT	Not functional
POWER SUPPLIES	
1A1A3PS1	
INT	On
EXT	On
1A1A3PS2	
INT	On
EXT	On
1A1A3PS3	
INT	On
EXT On	
1A1A3PS4	
INT	On
EXT	On
1A1A3PS5	
INT	On
EXT	On
1A1A3PS6	
INT	On
EXT	On

Table 3-8. ADP Lamp Test Indications - Continued

Indicator	Indication
1A1A3A5PS1	
INT	On
EXT	On
1A1A3A6PS1	
INT	On
EXT	On
1A1A3A7PS1	
INT	On
EXT	On
1A1A3A8PS1	
INT	On
EXT	On
BACKUP CONTROL CARDS	
1A13A5A1127	
Fault Indicator	On
1A1A3A6A1127	
Fault Indicator	On
1A1A3A7A1127	
Fault Indicator	On
1A13A8A1127	On
Fault Indicator	On

Table 3-9. Buffer Unit 1A1A3A2 Circuit Card Functional Groups

Device address	Buffer section (functional group)	MTS-testable cards	Nontestable cards
01_	IOX 1	A1427 thru A1431 A1434 thru A1445	A1432, A1446
02_	IOX 2	A1327 thru A1331 A1334 thru A1345	A1332, A1346
10_	IOE 0	A1313 thru A1317	A1318
11_	IOE 1	A1320 thru A1324	A1325
12_	IOE 2	A1406 thru A1410	A1411
13_	IOE 3	A1413 thru A1417	A1418
14_	IOE 4	A1420 thru A1424	A1425

CHAPTER 4
REMOVAL AND REPLACEMENT PROCEDURES AND CABLING/WIRING DIAGRAMS

Section I. REMOVAL AND REPLACEMENT PROCEDURES

4-1. Scope This section provides procedures for onsite removal and replacement of equipment rack 1A1A2 and 1A1A3 components of the ADP equipment. It also provides procedures for removal and replacement of common front-panel-mounted components such as panel indicator lamps, switches, and indicator. For removal and replacement of the ADP interface and external interface panels, refer to TM 9-1430-655-20-1.

4-2. Panel Indicator Lamp Removal and Replacement (fig. 4-1).

CAUTION

If replacement lamps are not available, do not remove defective lamps. Vacant lamp positions In the lens assembly can cause short-circuiting.

a. *Removal.* To remove a panel indicator lamp, proceed as follows:

(1) Pull lens assembly (1) containing faulty indicator lamp from socket (2).

(2) Unscrew chrome retaining knob (3) ccw to separate lens assembly (1).

(3) Pull defective lamp (4) from lens assembly(1).

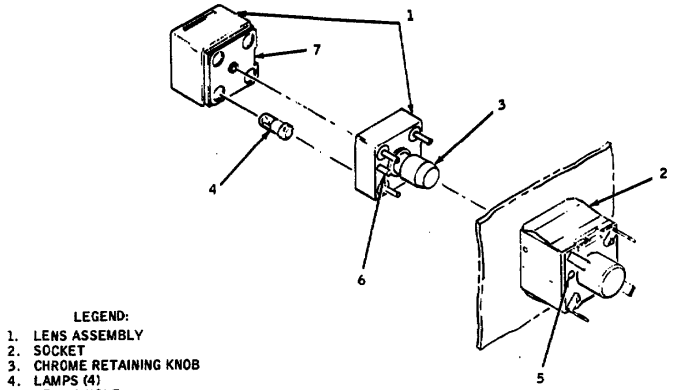
b. *Replacement.* To replace a panel indicator lamp, proceed as follows:

(1) Insert replacement lamp (4) in lens assembly (1).

(2) Position alinement notches (7) on separated parts of lens assembly, and reassemble lens assembly (1).

(3) Tighten chrome retaining knob (3) cw to secure lens assembly (1) together.

(4) Position lens assembly keying pin (6) with keying hole (5) in socket (2), and press lens assembly (1) firmly into socket.



LEGEND:
1. LENS ASSEMBLY
2. SOCKET
3. CHROME RETAINING KNOB
4. LAMPS (4)
5. KEYING HOLE
6. KEYING PIN
7. ALINEMENT NOTCH

MS 202439

Figure 4-1. Panel Indicator Lamp ,Removal and Replacement

4-3. Indicator Switch Lamp Removal and Replacement (fig. 4-2).

CAUTION

If replacement lamps are not available, do not remove defective lamps. Vacant lamp positions in the lens assembly can cause short-circuiting.

a. *Removal*. To remove an indicator switch lamp, proceed as follows:

(1) Using a small screwdriver, move latch (1) to right until lens assembly (2) releases forward from indicator switch socket (3).

(2) Rotate lens assembly (2), up to 90 degrees, to disengage lens assembly shaft (4) from socket hole (9).

(3) Separate lens assembly (2) from socket (3).

(4) Reinsert lens assembly shaft (4) into socket hole (9) and unscrew lens assembly shaft (4) by turning lens assembly ccw . Separate lens assembly (2).

(5) Remove defective lamp (5) from lens assembly (2).

b. *Replacement.* To replace an indicator switch lamp, proceed as follows:

(1) Insert replacement lamp (5) in lens assembly (2).

(2) Using indexing notches (6), aline separate parts of lens assembly (2), and reassemble lens assembly.

CAUTION

Do not overtighten the lens assembly shaft, or damage to the lens assembly housing can occur. Tighten it just enough to secure the lens assembly firmly together.

(3) Replace lens assembly shaft (4) to secure lens assembly (2) together.

(4) Insert lens assembly (2) with lens assembly shaft (4) into socket hole (9). Rotate lens assembly (2), up to 90 degrees, until lens assembly shaft (4) slides into socket hole (9). Continue to rotate lens assembly (2) until latch (1) alines with cutout on bottom side of lens assembly. Press lens assembly (2) into socket (3) until it locks into place.

4-4. Indicator Switch Mechanism Removal and Replacement (fig. 4-2).

a. *Removal.* To remove an indicator switch, proceed as follows:

(1) On ADP STATUS AND CONTROL panel, set POWER ADP switch to OFF.

(2) Using small screwdriver, move latch (1) to right until lens assembly (2) releases forward from indicator switch socket (3).

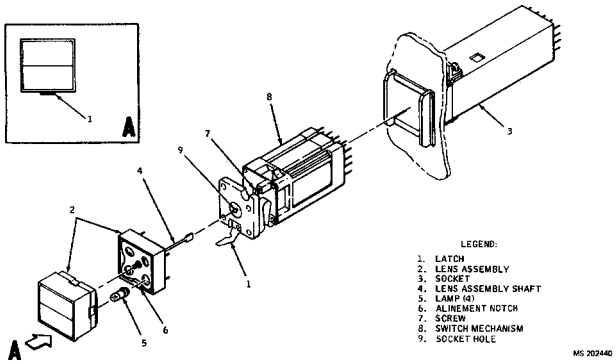


Figure 4-2. Indicator Switch Removal and Replacement

(3) Rotate lens assembly (2), up to 90 degrees, to disengage lens assembly shaft (4) from socket hole (9).
(4) Separate lens assembly (2) from socket (3).

(5) Using small-bladed screwdriver, turn screw (7) one-quarter turn ccw.

(6) Insert flat portion of lens assembly shaft (4) into socket hole (9).

(7) Using lens assembly (2) and shaft (4) as an extraction tool, pull switch mechanism (8) out of socket (3). Separate lens assembly (2) from switch mechanism (8).

b. *Replacement.* To replace an indicator switch mechanism, proceed as follows:

(1) Using small-bladed screwdriver, turn screw (7) one-quarter turn ccw.

(2) Orient replacement switch mechanism with latch (1) down and insert it into socket (3). With finger, press switch mechanism (8) into socket (3) until it locks in place.

(3) Insert lens assembly (2) with lens assembly shaft (4) into socket hole (9). Rotate lens assembly (2), up to 90 degrees, until lens assembly shaft (4) slides into socket hole (9). Continue to rotate lens assembly (2) until latch (1) alines with cutout on bottom side of lens assembly. Press lens assembly (2) into socket (3) until it locks into place.

(4) On ADP STATUS AND CONTROL panel, set POWER ADP switch to on (up).

4-5. Thumbwheel Switch, Removal and Replacement (fig. 4-3).

a. *Removal.* To remove thumbwheel switch, proceed as follows:

(1) On dc power panel, set applicable circuit breaker to OFF position.

(2) Check that POWER indicator for applicable unit is off.

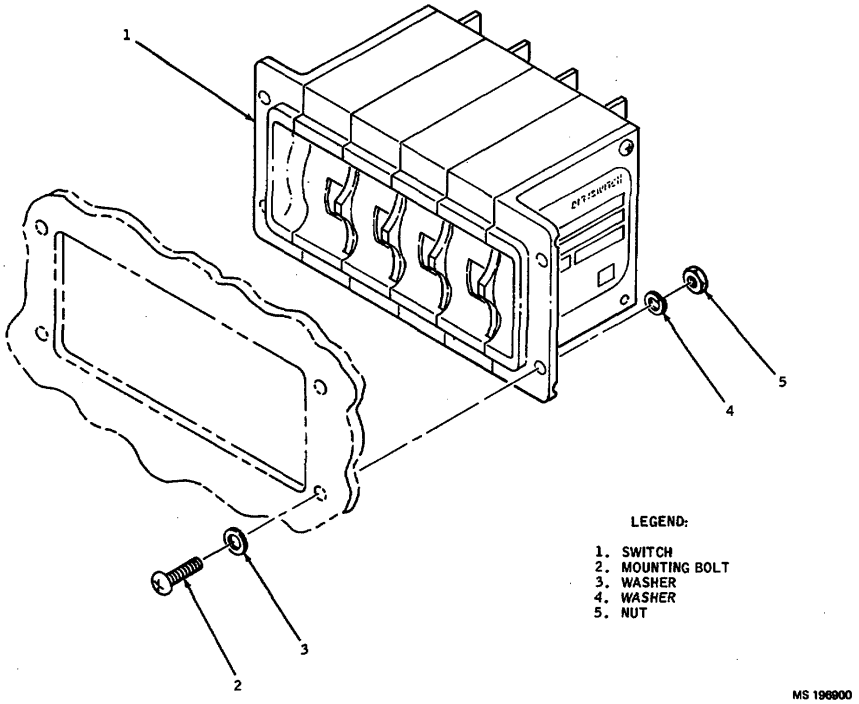


Figure 4 -3. Thumbwheel Switch, Removal and Replacement

CAUTION

Remove switch wires carefully, since the same wires will be used on replacement switch.

(3) Tag and disconnect wires from switch. For soldered connections, use a soldering iron of 40 watts maximum.

(4) Remove mounting bolts (2), washers (3 and 4), and nuts (5). Remove switch from front panel.

(5) Remove retaining clip (multiple switches only). Replace faulty switch section with replacement switch section.

b. *Replacemen*t. To replace thumbwheel switch, proceed as follows:

(1) Replace retaining clip (multiple switches only) and replace switch in panel.

(2) Install mounting bolts (2), washers (3 and 4), and nuts (5) to secure switch on panel.

(3) Reconnect wires to applicable terminals.

(4) Remove tags from wires.

(5) Verify switch operation by exercising switch functions.

(6) On dc power panel, set applicable circuit breaker to ON position.

4-6. Rotary Switch, Removal and Replacement (fig. 4-4).

a. *Removal*. To remove rotary switch, proceed as follows:

(1) On power control panel, set applicable circuit breaker to OFF position.

(2) Check that POWER indicator for applicable unit is off.

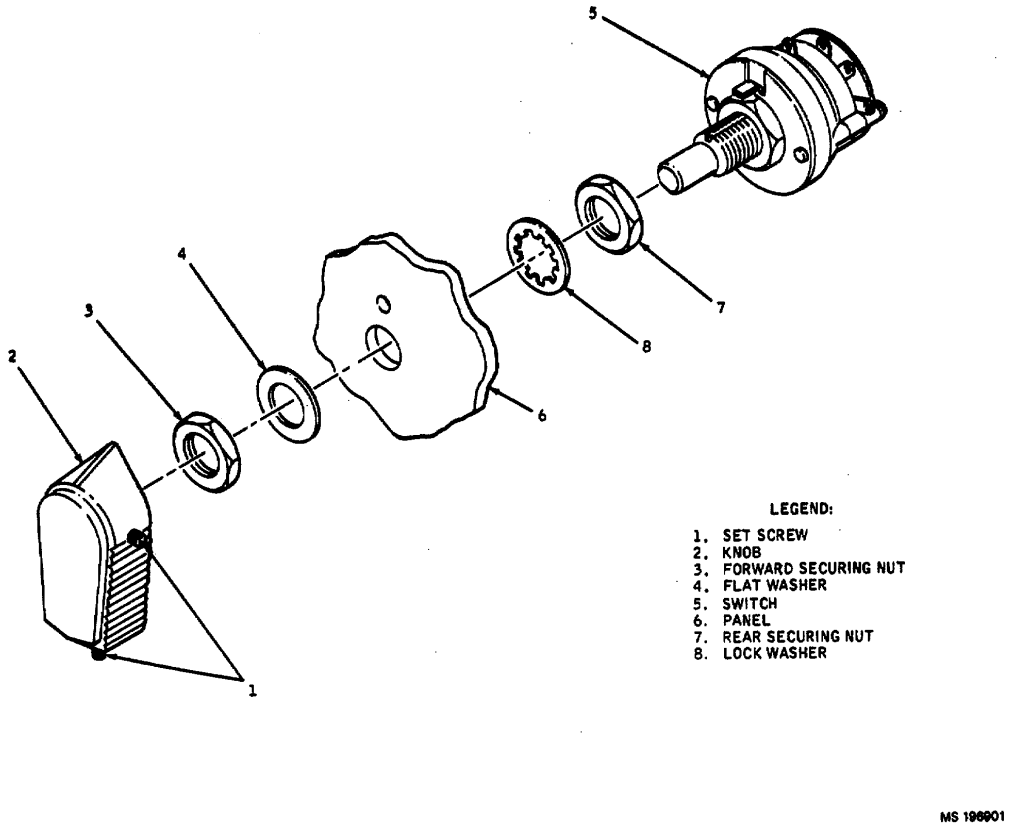


Figure 4 -4. Rotary Switch, Removal and Replacement

CAUTION

Remove switch wires carefully, since the same wires will be used on replacement switch.

(3) Locate rear portion of faulty switch.

(4) Tag and remove wires from rear of switch using soldering iron (40 watts maximum).

(5) Loosen set screws (1) and remove knob (2).

(6) Unscrew and remove forward securing nut (3). Remove keyed flat washer (4) from switch shaft.

(7) Remove switch (5) from rear of panel (6).

b. *Replac*ement. To replace rotary switch, proceed as follows:

(1) Prepare replacement rotary switch by screwing rear securing nut (7) on switch shaft followed by lockwasher (8).

(2) Insert replacement switch into panel hole from the rear.

(3) Install keyed flat washer (4) and screw forward securing nut (3) on switch shaft until one and one half threads are visible beyond the nut.

(4) Adjust position of switch until key portion of the keyed flat washer (4) fits in slot in panel.

(5) Tighten rear securing nut (7) until switch is secured to panel.

(6) Using soldering iron (40 watts maximum), solder tagged wires to applicable terminals.

(7) Replace knob (2) and aline to position of switch setting.

(8) Tighten set screws (1) until knob is secure on shaft.

(9) Check mechanical action of switch and correct alinement of knob.

(10)Close and secure panel.

(11)On power control panel, set applicable circuit breaker to ON position.

(12)Verify switch operation by exercising switch functions.

4-7. Toggle Switch (Lever Lock), Removal and Replacement (fig. 4-5).

a. *Removal.* To remove toggle switch, proceed as follows:

WARNING

Be sure that dc power circuit breaker for affected equipment is set to the OFF position to prevent shock hazard to personnel.

(1) Remove power from unit by setting respective circuit breaker on power control panel to the OFF position.

(2) Check that POWER indicator for affected unit is off.

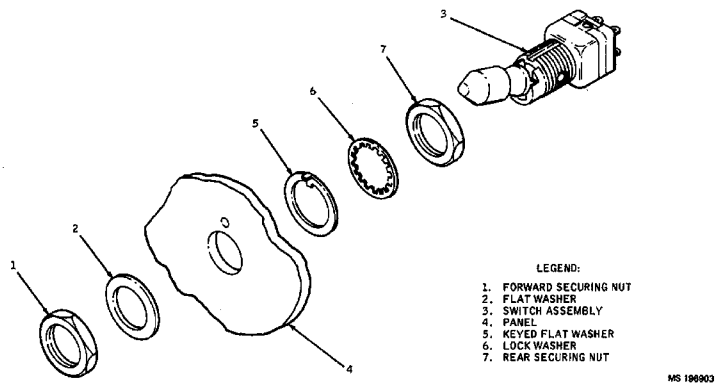


Figure *4-5. Toggle Switch (Lever Lock) Removal and Replacement*

CAUTION

Care must be taken during removal of switch wires, since the same wires will be used on replacement switch.

(3) Locate rear portion of switch

(4) Tag and remove wires from rear of switch using soldering iron (40 watts maximum).

(5) Unscrew and remove forward securing nut (1) and flat washer (2) from switch shaft.

(6) Remove switch (3) from rear of panel (4) and retain hardware.

b. *Replacement* To replace toggle switch, proceed as follows:

(1) Prepare replacement switch by screwing rear securing nut (7) on switch shaft followed by lock washer (6) and keyed flat washer (5).

(2) Insert replacement switch into panel hole from the rear.

(3) Install flat washer (2) and screw forward securing nut (1) onto switch shaft until one and one-half threads are visible beyond the nut.

(4) Adjust position of switch until key portion of the keyed flat washer (5) fits into slot in panel.

(5) Tighten rear securing unit (7) until switch is secure to panel.

(6) Connect and solder tagged wires to replacement switch and remove tags.

(7) Close and secure panel.

(8) On power transfer panel, set POWER SOURCE SELECT switch to TAC POWER or CONV POWER as applicable, then press SYSTEM POWER ON switch until indicator lights. Restore power to unit by placing respective circuit breaker and EMERGENCY POWER BATTERY OUTPUT circuit breaker on power control panel to the ON position.

4-7.1. 32K Memory Unit Wiring Harness W1, Removal and Replacement (fig. 4-5.1).

a. *Removal.* To remove wiring harness W1 (1), proceed as follows:

WARNINGS

The dc/dc converter (2) may be hot enough to cause burns. Keep hands clear when working near it.

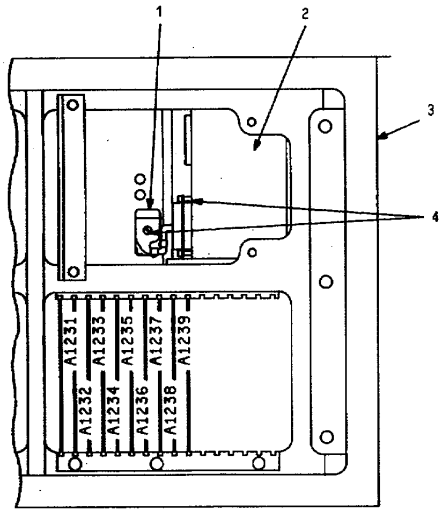


Figure 4-5.1. 32K Memory Unit

CAUTION

Make sure that dc power circuit breaker and backup switch for the affected equipment is set to off (down) position to prevent possible damage to the ICs.

(1) Open cabinet door to gain access to wiring harness W1 (1) in memory unit (1A1A3) (3).

(2) Loosen jackscrews (4) securing connectors P1 and P2.

(3) Using jackscrews, carefully disconnect connectors P1 and P2 from jacks and remove wiring harness W1 (1).

b. *Replacement.* To replace wiring harness W1 (1) in memory unit, proceed as follows:

(1) Carefully insert connectors P1 and P2 fully into their respective jacks.

(2) Carefully tighten connector P1 and P2 jackscrews (4) for secure connector mating.

(3) Close cabinet door.

4-8. DC/DC Converter, Removal and Replacement (fig. 4-6).

a. *Removal.* To remove dc/dc converter, proceed as follows:

WARNING

Make sure that dc power circuit breaker and backup switch for the affected unit is off before attempting removal or replacement of the dc/dc converter. Observe all high voltage safety precautions. When power is on, high voltages in this area can be fatal.

(1) Remove power to affected unit by setting corresponding main power panel circuit breaker and the backup switch to OFF position.

(2) Place door(s) of affected rack in the maintenance position and locate applicable dc/dc converter.

(3) Disconnect cables to dc/dc converter J1 and J2.

WARNING

High case operating temperatures can cause handling difficulty. Keep hands clear when handling dc/dc converter. (4) Release four captive retaining screws and slide dc/dc converter straight out of rack.

b. *Replacement.* To replace dc/dc converter, proceed as follows:

CAUTION

Dc/dc converters must be reinstalled with attaching hardware properly torque to make sure that damage does not result from poor heat dissipation.

(1) Position replacement dc/dc converter and secure with four captive retaining screws.

(a) For equipment rack 3 front-door mounted dc/dc converter power supplies, torque retaining screws 13 to 16-inch-pounds.

(b) For equipment rack 3 rear door mounted dc/dc converter power supplies, torque retaining screws 7 to 9-inch-pounds.

(2) Connect cables to replacement dc/dc converter J1 and J2.

(3) Secure rack door(s).

(4) Restore power to affected unit by setting corresponding main power panel circuit breaker(s) to ON position.

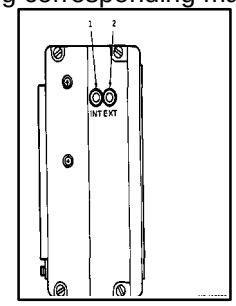


Figure 4-6. DC/DC Converter, Removal and Replacement

4-9. Circuit Card Assembly, Removal and Replacement (fig. 4-7).

CAUTION

CMOS memories contain electrostatic sensitive devices requiring special handling to avoid electrostatic discharge damage. When removing and replacing memory cards, observe the following precautions:

a. Immediately prior to handling within the shelter, make physical contact with a grounded surface to discharge any possible buildup of static electricity.

b. Package the memory storage card in electrostatic bags prior to removing from the shelter.

Make sure that dc power circuit breaker and backup switch for the affected equipment is set to off (down) position to prevent possibly damaging the ICs on the memory circuit cards.

a. *Removal*. To remove circuit card assembly, proceed as follows:

(1) Press spring-loaded card retainer locking pin (1), and slide card retainer bar to clear card edges.

CAUTION

Hold circuit card assembly with free hand before releasing grip on card extractor to prevent card damage.

(2) Engage card extractor (2) in holes on front of circuit card. Squeeze and hold card extractor grip and pull circuit card straight out of slot. Hold circuit card in free hand and release card extractor grip.

b. *Replacement*. To replace circuit card assembly, proceed as follows:

CAUTION

When circuit card is replaced, make sure component side of circuit card is to the left of the operator to prevent damage to circuit card or connector.

(1) Position replacement circuit card in slot by hand and press firmly to seat connector.
(2) Slide card retainer bar (4) into place until card retainer locking pin (1) engages.

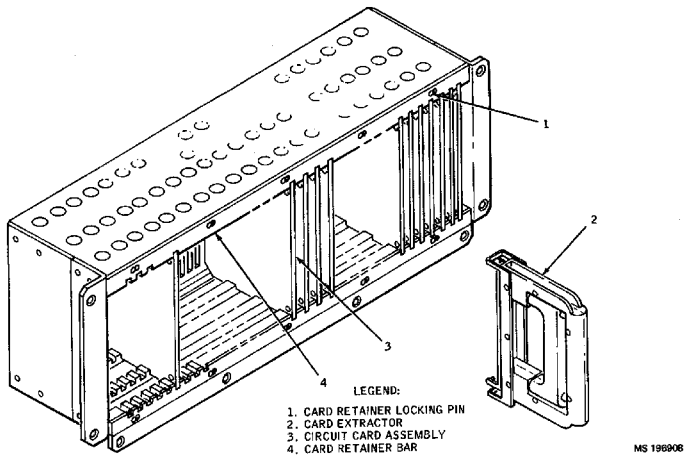


Figure 4-7. Circuit Card Assembly, Removal and Replacement

4-10. Card Retainer Removal and Replacement.
Card retainers supplied with replacement card cages are not color coded as to circuit card types (para 3-10). To avoid color coding the card retainers on replacement card cages, substitute the card retainers from the card cage to be replaced with the card retainers on the replacement card cage. To substitute the card retainers, proceed as follows:

a. On replacement card cage, remove screws attaching card retainers to card cage and remove all card retainers from card cage.
b. On card cage to be replaced, remove card retainers one at a time and install in corresponding locations on replacement card cage. Tighten attaching screws so that card retainer will slide smoothly on mounting surface.
c. Install blank card retainers on replaced card cage.

4-11. Application of Color Disks to Card Retainers.
To apply color disks to card retainers, proceed as follows:

a. Clean card retainer surface to which color disk is to be applied with a clean lint-free cloth dampened with perchloroethylene solvent (Federal Specification O-P-191 or equivalent). While surface is still wet, wipe dry with a clean, dry, lint-free cloth.
b. Refer to para 3-10 and determine color of color disk to be applied.
c. Refer to figure 3-3 for zone location of color disk and apply color disk to card retainer. When applying color disk to card retainer, avoid touching color disk adhesive or card retainer surface.
d. Apply a protective coating of transparent tape or epoxy resin over color disk and mounting surface. Use transparent tape conforming to MIL-I-15126 type MFT 2.5 or 3.5 or epoxy resin conforming to MIL-A- 8623.

4-12. Upper Central Processor Unit Bay 1 1A1A3A3 and Lower Central Processor Unit Bay 1 1AlA3A4 Card Cage, Removal and Replacement (fig. 4-8).

a. *Removal.* To remove upper and lower CPU card cages in bay 1, proceed as follows:

WARNING

Make sure main power to the applicable card bay is off. If possible, turn off all power except that for lighting and air-conditioning before attempting this procedure to reduce shock hazard to personnel.

Two men are required to remove the card cages to prevent injury to personnel or damage to the equipment.

(1) Gain access to card side of card cage (1) by opening rack door(s) to maintenance position (s).
(2) Disconnect wiring harness connectors from card bay.

NOTE

Card extractor tool must be used for ribbon cable connectors.

(3) Remove two screws securing front panel stop and remove stop.
(4) Remove securing screws (2) and cap screws (3) from bay 2 (4) and swing open.
(5) Remove four mounting screws (5) from rear (right side) of card cage (1).
(6) Remove four mounting screws (6) and cap screws (7) from front (right side) of card cage. Remove card cage to maintenance bench.
(7) Transfer card assemblies from removed card cage to replacement card cage.

NOTE

If card cage is to be replaced with a replacement card cage, refer to para 4-11 and exchange card cage card retainers.

b. *Replacement.* To replace upper and lower CPU card cages in bay 1, proceed as follows:

(1) Position replacement card cage in housing. Secure four screws from front (right-side).
(2) Secure two screws from rear (right side) of card cage.
(3) Secure front panel stop with two screws.

(4) Close bay 2 and secure.

(5) Connect wiring harness connectors to replacement card cage.

(6) Close and secure rack door(s).

4-13. Upper Central Processor Unit Bay 2 1A1A3A3 and Lower Central Processor Unit Bay 2 1A1A3A4 Card Cage, Removal and Replacement (fig. 4-9).

a. *Removal*. To remove upper and lower CPU card cages in bay 2, proceed as follows:

WARNING

Two men are required to remove the card cages to prevent injury to personnel or damage to the equipment.

(1) Gain access to card side of card cage (1) by placing rack door (s) in maintenance position (s).

(2) Disconnect wiring harness connectors from card bay.

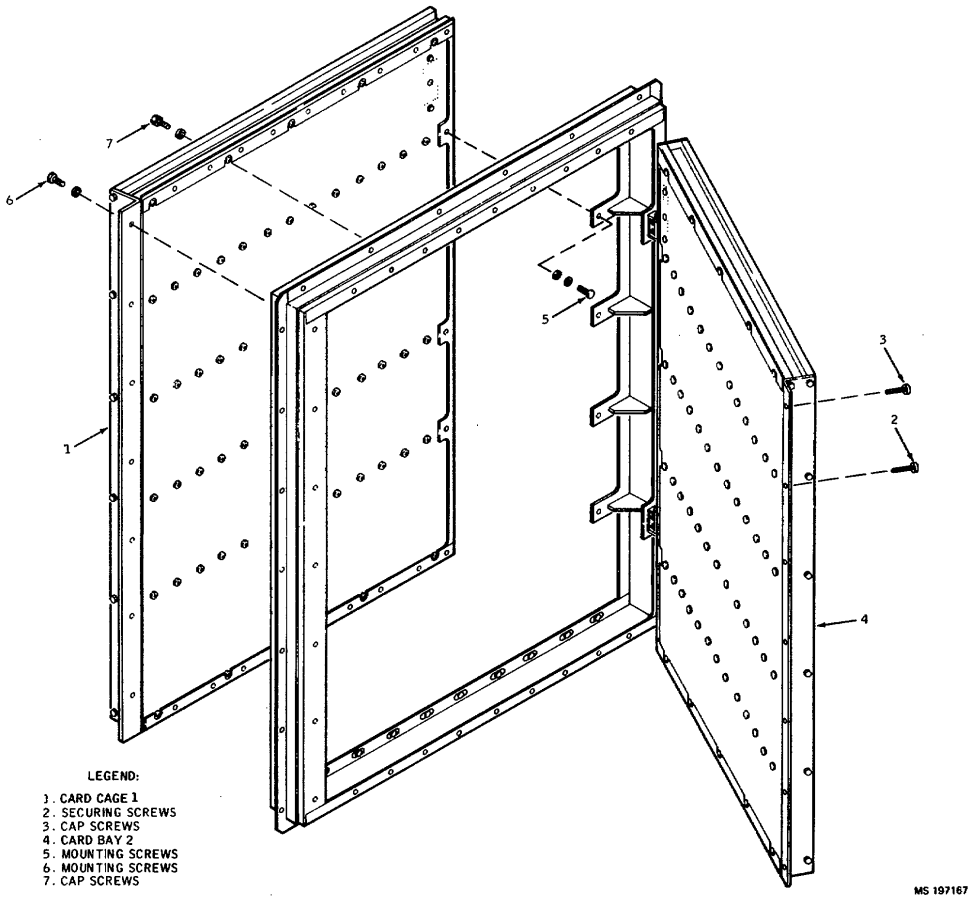


Figure 4-8. Upper Central Processor Unit Bay 1 1A1A3A3 and Lower Central Processor Bay 1 1A1A3A4 Card Cage, Removal and Replacement

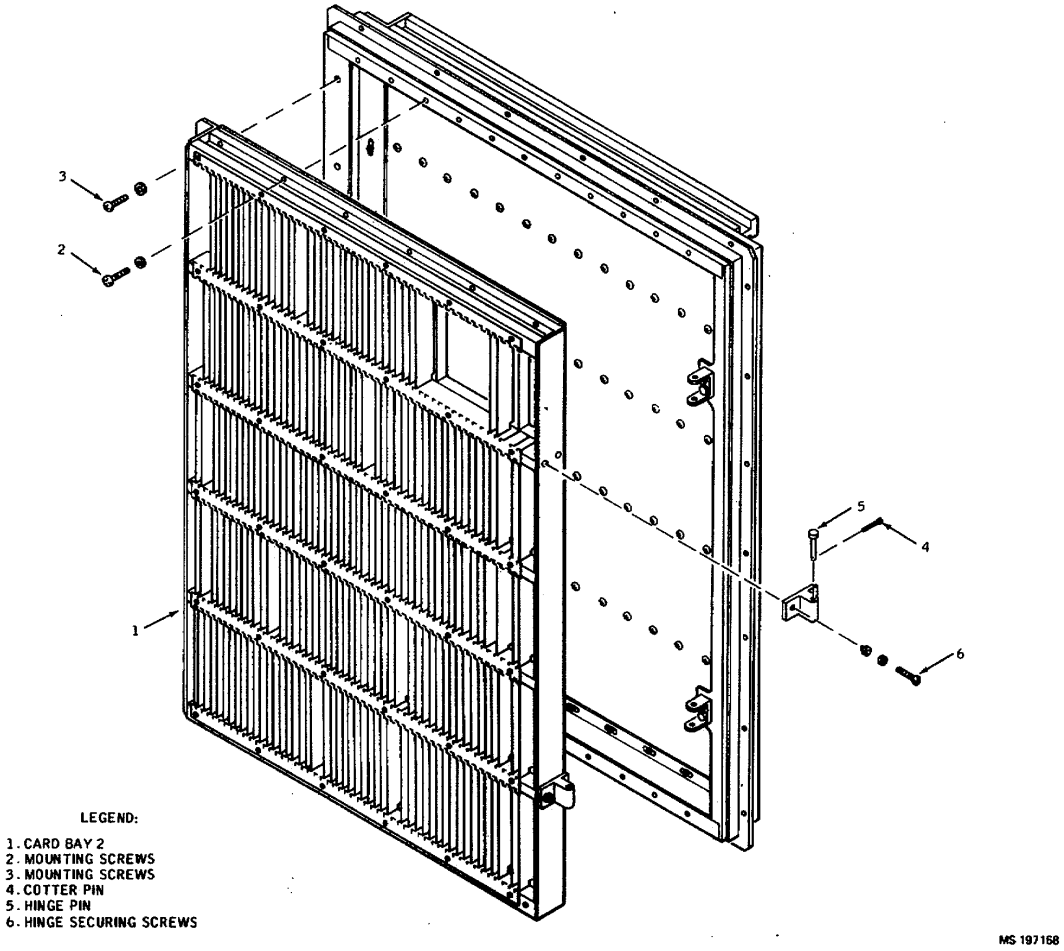


Figure 4-9. Upper Central Processor Unit Bay 2 1A1A3A3 and Lower Central Processor Unit Bay 2 1A1A3A4 Card Cage, and Replacement

NOTE

Card extractor tool must be used for ribbon cable connectors.

(3) Remove mounting screws (2) from top and bottom of card cage.
(4) Remove mounting screws (3) from side opposite hinges.
(5) Remove cotter pins (4) and hinge pins (5). Remove card cage to maintenance bench.
(6) Transfer card assemblies from card cage.
(7) Remove four screws (6) securing hinge halves to removed card cage. Secure hinge halves to replacement card cage.

NOTE

If card cage is to be replaced with a replacement card cage, refer to para 4-11 and exchange card cage card retainers.

b. *Replacement* To replace upper and lower CPU card cages in bay 2, proceed as follows:

(1) Position replacement card cage in housing. Replace hinge pins and cotter pins.
(2) Secure mounting screws (2 and 3).
(3) Connect wiring harness cable connectors to replacement card bay.
(4) Secure rack door(s).

4-14. Input/Output Unit 1A1A3A1 and Buffer Unit 1A1A3A2 Card Cage, Removal and Replacement (fig. 4-10).

a. Removal To remove IOU and buffer unit card cages, proceed as follows:

WARNING

Two men are required to remove the card cages to prevent injury to personnel or damage to the equipment.

(1) Gain access to card side of card cage.
(2) Disconnect wiring harness connectors and power connector from card bay.

NOTE
Card extractor tool must be used for ribbon cable connectors.

(3) Gain access to wire wrap side of card cage.

(4) Remove screws (2) on left edge of wire wrap side of card cage. Use offset screwdriver, if necessary.
(5) Remove mounting screws (3 and 4) from left edge and top and bottom of card side of card cage. Remove bay to maintenance bench.
(6) Transfer card assemblies from removed card cage to replacement card cage.

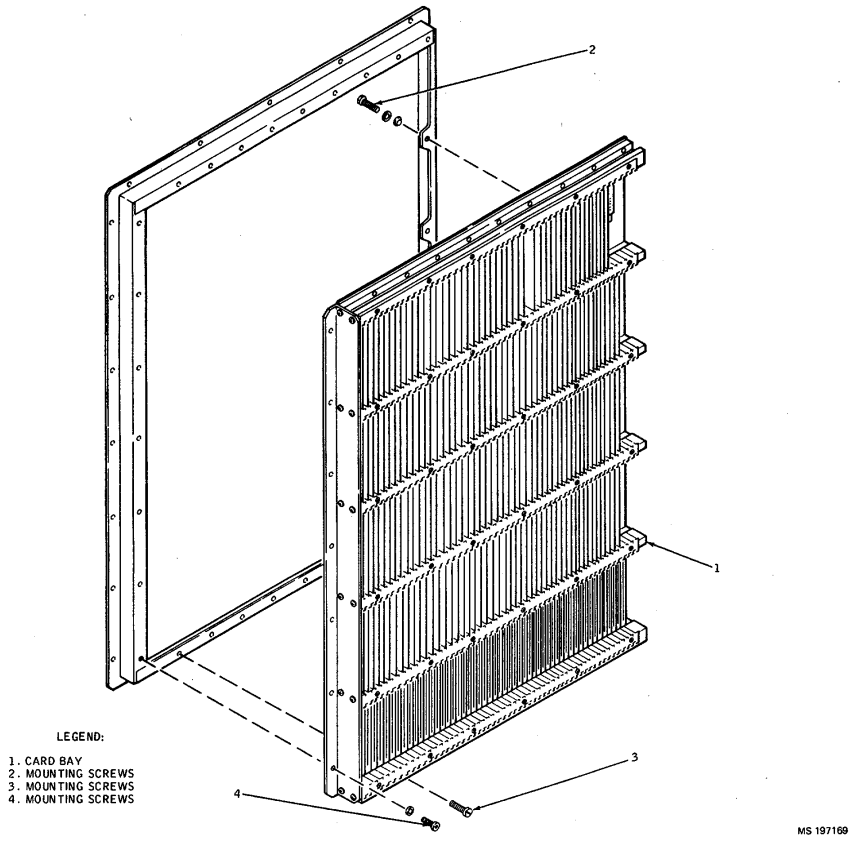


Figure 4-10. Input/Output Unit 1A1A3A1 and Buffer Unit 1A1A3A2 Card Cage, Removal and Replacement

b. *Replacement* To replace IOU and buffer unit card cages, proceed as follows:

(1) Position replacement card cage in housing.
(2) Secure card cage (wire wrap side first) with removed attaching parts.
(3) If removed, position and secure blank access panel to lower portion of rack door.
(4) Connect wiring harness and power connectors to card bay.
(5) Close and secure rack door.

4-15. 32K Memory Unit, Removal and Replacement (fig. 4-11).

CAUTION

CMOS memories contain electrostatic sensitive devices requiring special handling to avoid electrostatic discharge damage. When removing and replacing memory cards, observe the following precautions:

a. Immediately prior to handling within the shelter, make physical contact with a grounded surface to discharge any possible buildup of static electricity.

b. Package the memory storage card in electrostatic bags prior to removing from the shelter.

Make sure that dc power circuit breaker and backup switch for the affected equipment is set to off (down) position to prevent possibly damaging the ICs on the memory circuit cards.

a. *Removal.* To remove 32K memory units, proceed as follows:

(1) Gain access to card side of memory unit (3) by opening rack door to maintenance position.

NOTE

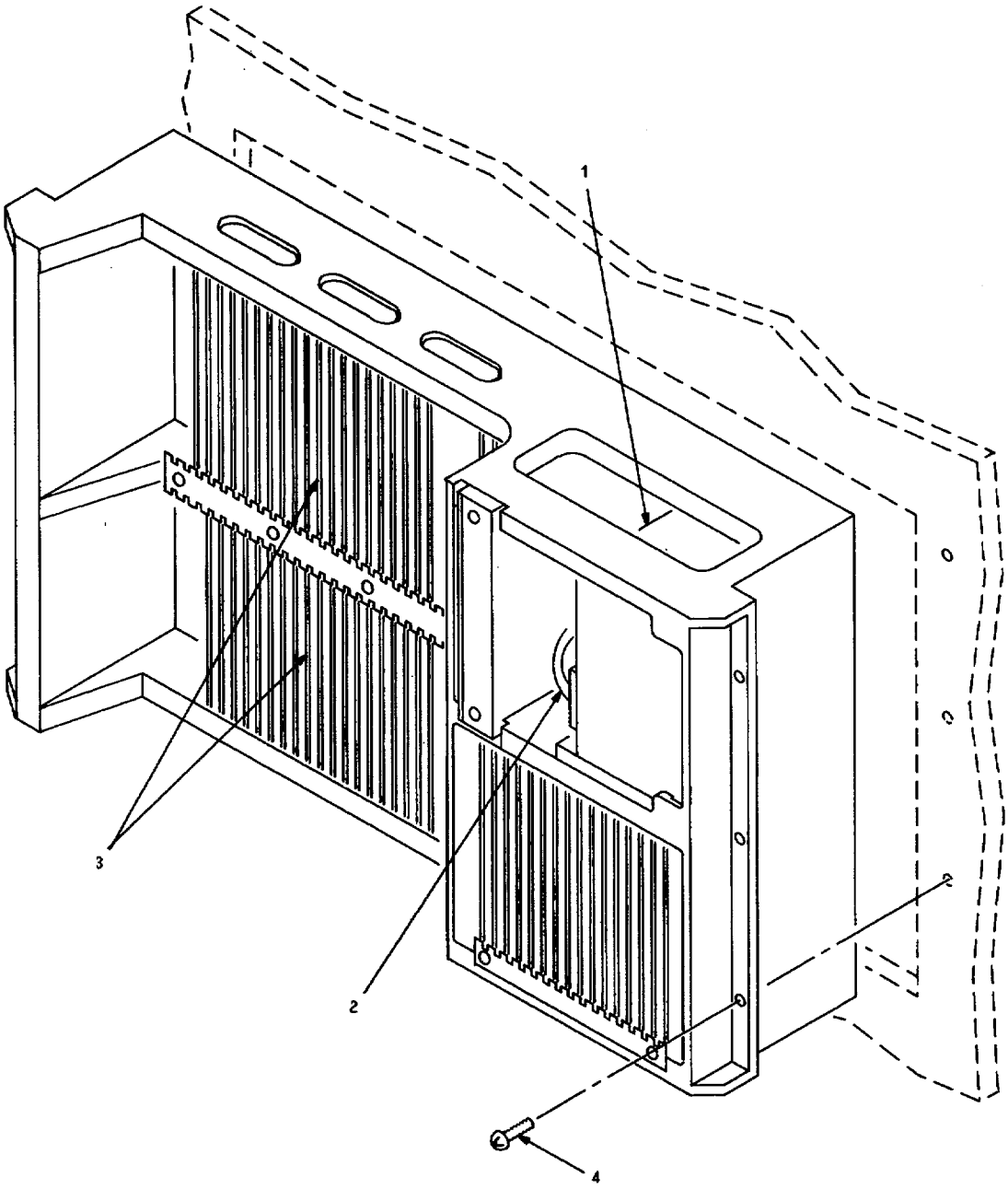
Card extractor tool must be used for ribbon cable connectors.

(2) Disconnect ribbon cable connectors from memory unit (3).
(3) Disconnect W477 from connector J2of dc/dc converter (1).
(4) Remove six mounting screws (4). Pull memory unit (3) from housing.
(5) Transfer card assemblies from removed memory unit to replacement memory unit.
(6) Transfer wiring harness (2) from removed unit to replacement unit in accordance with procedures in paragraph 4-7.1.
(7) Transfer dc/dc converter (1) from removed unit to replacement unit in accordance with procedures in paragraph 4-8.

b. *Replacement.* To replace 32K memory unit, proceed as follows:

(1) Position replacement memory unit (3) in housing and secure with six mounting screws (4).
(2) Connect ribbon cable connectors to replacement card bay.
(3) Connect W477 to connector J2 of dc/dc converter (1).
(4) Close and secure rack door(s).

4-16. Deleted.



LEGEND:

1. DC/DC CONVERTER
2. WIRING HARNESS
3. MEMORY UNIT
4. MOUNTING SCREW (6)

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Figure 4-11. 32K Memory Unit, Removal and Replacement

Section II. CABLING AND WIRING DIAGRAMS

4-17. General. This section contains signal and power cabling diagrams for the ADP equipment. All electrical interconnections between the equipments are made with the cables shown in figure 4-12. Although the ADP interface panel is not considered part of the ADP equipment, it is included here because all ADP cable interconnections are made through this panel. Also included in this section is a power distribution diagram for the ADP equipment.

4-18. Signal Cabling. Figure 4-12 is a signal cabling diagram for the ADP equipment. All ADP equipment signal cables are wired pin-to-pin. For example, pin A of plug P1 is wired to pin A of plug P2, and so on. For details on the signal cables, refer to the cable wiring diagrams in Overall System Maintenance Manual TM 9-1430-655-20-1.

4-19. Power Cabling. Figure 4-13 is an IOX cabling diagram for the ADP equipment. ADP equipment power cables are wiring harnesses and are not wired pin-to-pin. Table 4-1 lists the power cables and the wire lists which define the cable interconnections. Figure 4-14 is a cabling diagram for the ADP equipment power supply. The wire lists are contained in the wire lists manual. Instructions on use of the wire lists are contained in Overall System Maintenance Manual TM 9-1430-655-20-1.

Table 4-1. ADP Equipment Power Cables

Cable	Wire list
W477	WL13143814
W478	WL10282617
W537	WL13143813
W1*	WL13143804

*W1 is located in four places: 1A1A3A5 thru 1A1A3A8.

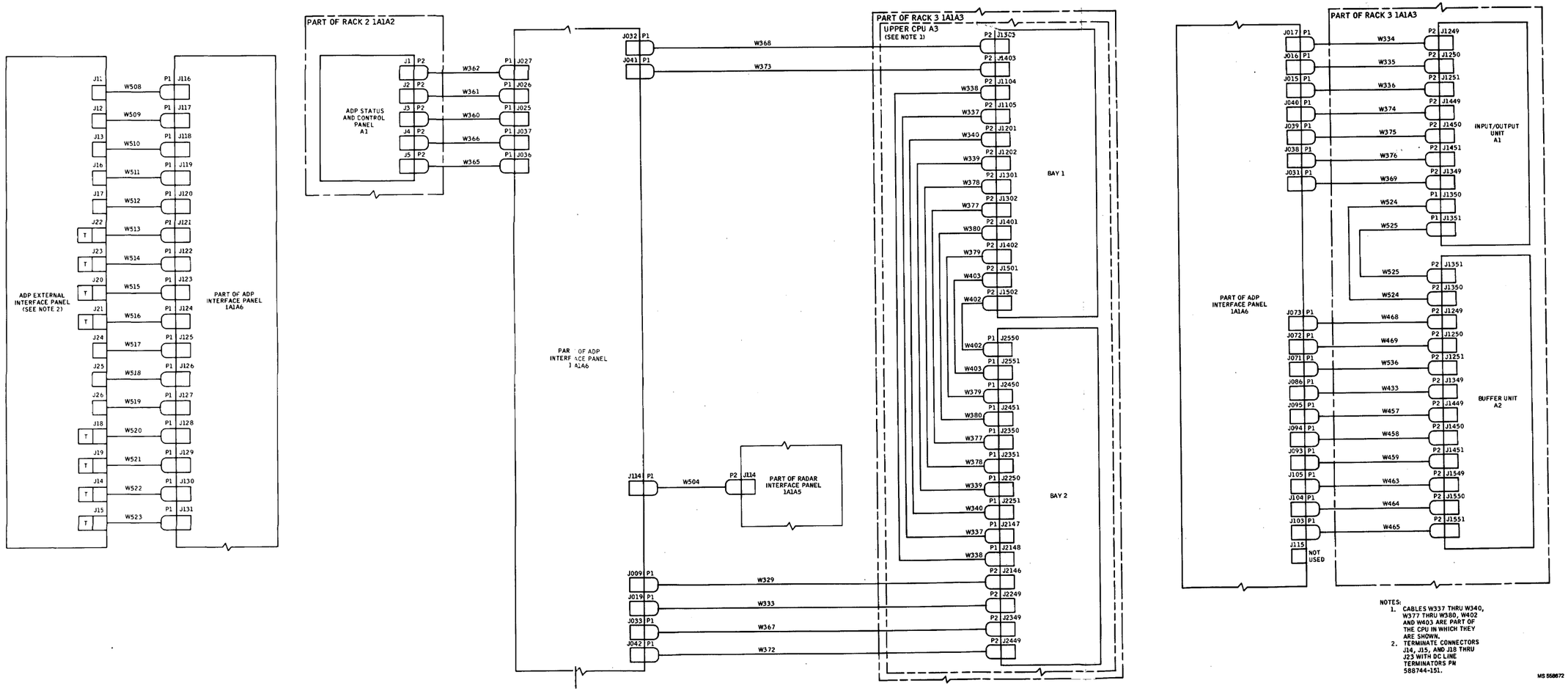

Figure 4-12. ADP Equipment Signal Cabling Diagram (Sheet 1 of 2)

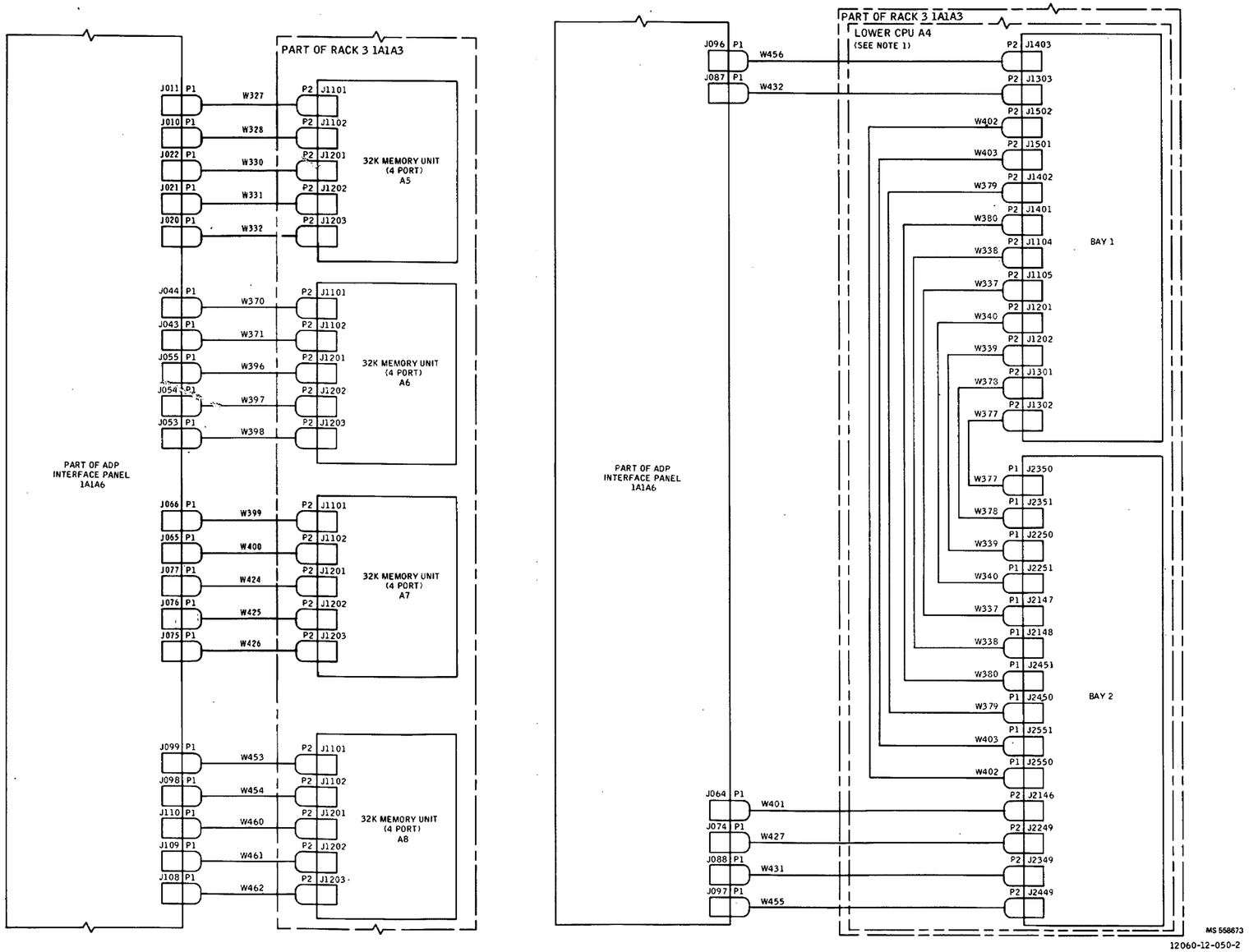

Figure 4-12. ADP Equipment Signal Cabling Diagram (Sheet 2 of 2)

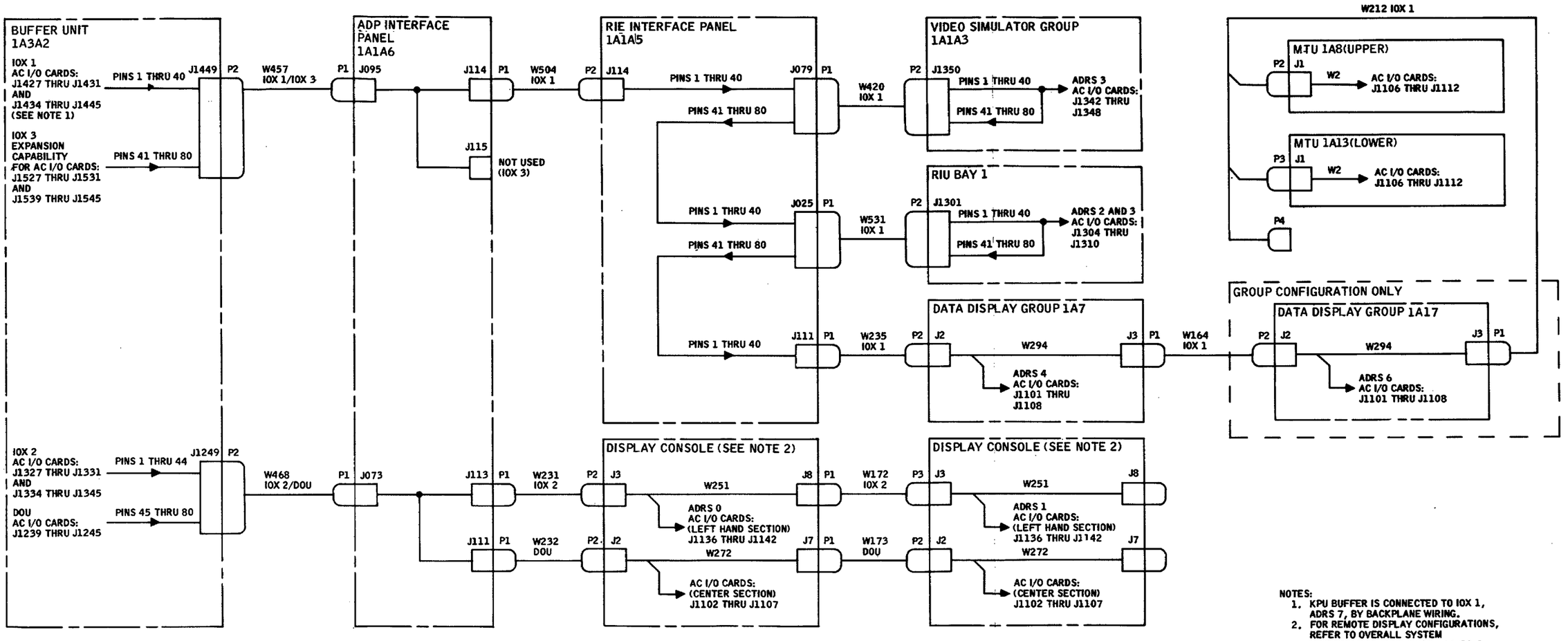

Figure 4-13. Input/Output Exchange (IOX) Cabling Diagram

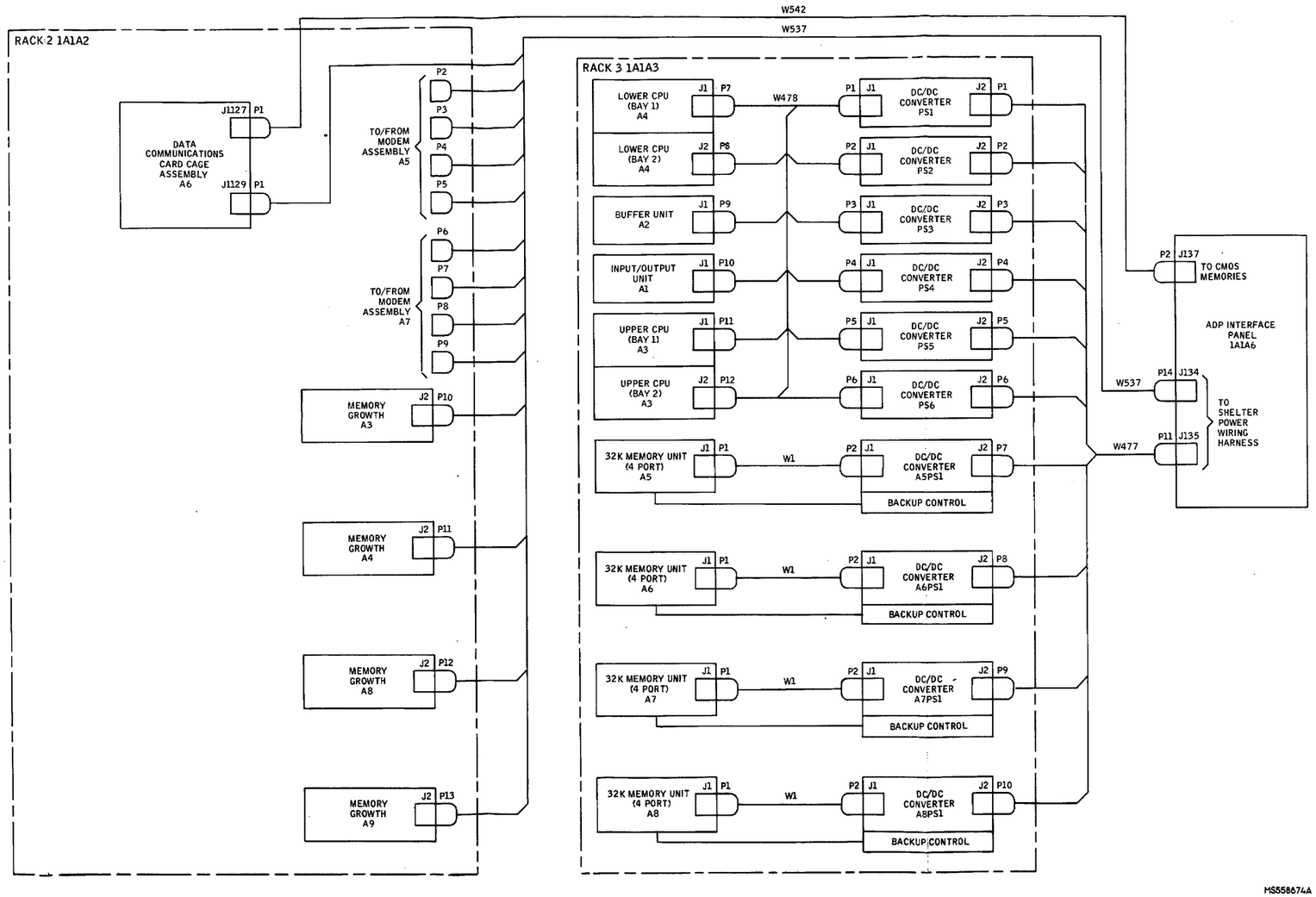

Figure 4-14. Automatic Data Processor Equipment Power Supply, Cabling Diagram

APPENDIX A

LIST OF ABBREVIATIONS

ACM	Automatic Clutter Mapper (part of Video Processor Unit)
ACP	Azimuth Change Pulse
ADIZ	Air Defense Identification Zones
ADP	Automatic Data Processor
ANP	Azimuth North Pulse
AP	Alterable Processor (part of display console)
ARO	Auxiliary Read-Out (part of CRT display)
ASCII	American Standard Code for Information Interchange
ASRT	Advance Support Radar Team (Marines)
ATDS	Air Tactical Data Systems (Navy)
ATMAC	Air Traffic Management Automated Center (Army)
BAMS	Binary Angular Measurement System
BITE	Built-In Test Equipment (part of Video Processor Unit)
BL	Block Length
BOT	Beginning Of Tape
Byte	Part of a data word, normally consisting of 8 bits
CBR	Chemical, Biological, Radiological (warfare, environment)
CFAR	Constant False Alarm Rate (part of video processor unit)
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processor Unit (part of ADP)
DASC	Direct Air Support Center (Marines, Air Force)
DC	Display Controller (part of display console)
DDG	Data Display Group
DEX	Device Command and Exit
DF	Display File
DEFK	Differential Frequency Shift Keying
DG	Display Generator (part of display console)
DOU	Display Output Unit (part of ADP)
DRF	Display Refresh File (DF)
ECP	Environmental Control Panel
EOB	End-of-Block
EOF	End-of-File
EOT	End of Tape
EPL	Error Program Level
EST	Equipment Status Table

FACP	Forward Air Control Part (Air Force)
FD	Fault Detection
FI	Fault Isolation
FPU	Forward Participating Unit
FSK	Frequency Shift Keying
FU	Fire Unit
IBDL	Interim Battery Data Link
IC	Integrated Circuit
IIU	IFF Integration Unit (part of Radar Interface Equipment
I/O	Input/Output
IOC	Input/Output Controller
IOE	Input/Output Expander (part of input/output multiple:
IOM	Input/Output Multiplexer (part of ADP)
IOU	Input/Output Unit (part of ADP)
IOX	Input/Output Exchange (part of ADP)
IPE	Instruction Parity Error
IRG	Inter-Record Gap
ITR	Input-to-Register
KPU	Keyboard Printer Unit
KPUC	Keyboard Printer Unit Controller (part of KPU)
LED	Light-Emitting Diode
LRC	Longitudinal Redundancy Check
LSB	Least Significant Bit
MACCS	Marine Air Command and Control System
MBA	Memory Bank Assignment
M&D	Maintenance and Diagnostic (program)
MPU	Main Power Unit
MSB	Most Significant Bit
MTC	Magnetic Tape Cartridge
MTS	Module Test Set
MTT	Magnetic Tape Transport
MTU	Magnetic Tape Unit (part of ADP)
MU	Memory Unit
NPL	Normal Program Level
NTDS	Naval Tactical Data Systems
OFR	Output-from-Register
OP Code	Display Code for Character Generator

PAR	Program Activity Register
PCP	Power Control Panel (part of MPU)
PDP	Power Distribution Panel (part of MPU)
PSC	Programming Support Center
PPI	Plan Position Indicator (part of CRT display)
PTU	Power Transfer Unit (part of MPU)
PU	Participating Unit
QUAD	Quadruple
Radar Mile	2000 years or 12.36 microseconds
RAM	Random-Access Memory
RAMIT	Rate-Aided Manually-Initiated Tracking
RIE	Radar Interface Equipment
RIU	Radar Integration Unit (part of RIE)
RSU	Range Synchronizer Unit (part of RIE)
RTC	Real-Time Clock
RU	Reporting Unit
SDC	Synchro-to-Digital Converter (part of RIE)
SDP	Status Display Panel
SOC	Start-Of-Character
SOP	Standard Operating Procedure (using unit)
SU	Supporting Unit
TADIL	Tactical Digital Information Link
TD	Target Detector (part of Video Processor Unit)
TDS	Target Detector Selector (part of Video Processor Unit)
TEWA	Threat Evaluation and Weapon Assignment
TMON	Test Monitor
TOS	Tactical Operations System (Army)
TP	Target Processor (part of Video Processor Unit)
VC	Video Compressor (part of display console)
VCC	Voice Communications Central
VCS	Voice Communications Station
VPU	Video Processor Unit (part of RIE)
VSU	Video Simulator Unit
XPL	Executive Program Level
32K MU	32K Memory Unit

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INDEX

INDEX - Continued

INDEX - Continued

INDEX - Continued

INDEX - Continued

INDEX - Continued

INDEX - Continued

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THE METRIC SYSTEM AND EQUIVALENTS

'NEAR MEASURE

. Centimeter = 10 Millimeters = 0.01 Meters = 0.3937 Inches
1 Meter = 100 Centimeters = 1000 Millimeters = 39.37 Inches
1 Kilometer = 1000 Meters = 0.621 Miles

'VEIGHTS

Gram = 0.001 Kilograms = 1000 Milligrams = 0.035 Ounces
1 Kilogram = 1000 Grams = 2.2 lb.
1 Metric Ton = 1000 Kilograms = 1 Megagram = 1.1 Short Tons

LIQUID MEASURE

1 Milliliter = 0.001 Liters = 0.0338 Fluid Ounces
1 Liter = 1000 Milliliters = 33.82 Fluid Ounces

SQUARE MEASURE

1 Sq. Centimeter = 100 Sq. Millimeters = 0.155 Sq. Inches
1 Sq. Meter = 10,000 Sq. Centimeters = 10.76 Sq. Feet
1 Sq. Kilometer = 1,000,000 Sq. Meters = 0.386 Sq. Miles

CUBIC MEASURE

1 Cu. Centimeter = 1000 Cu. Millimeters = 0.06 Cu. Inches
1 Cu. Meter = 1,000,000 Cu. Centimeters = 35.31 Cu. Feet

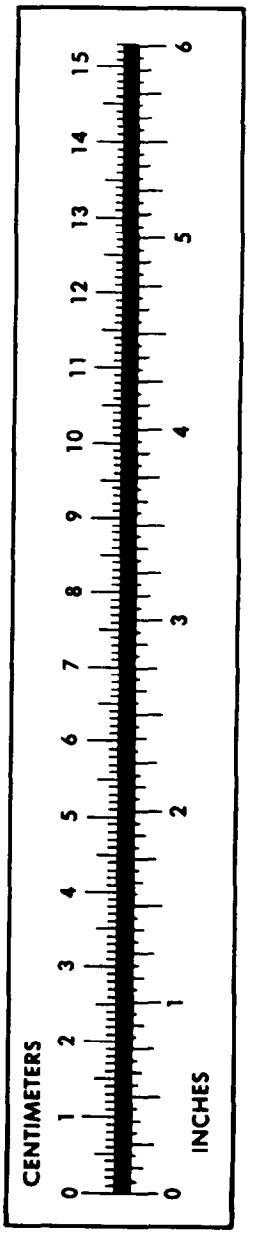
TEMPERATURE

5/9(°F - 32) = °C
212° Fahrenheit is evuivalent to 100° Celsius
90° Fahrenheit is equivalent to 32.2° Celsius
32° Fahrenheit is equivalent to 0° Celsius
9/5C° + 32 =°F

APPROXIMATE CONVERSION FACTORS

TO CHANGE	TO	MULTIPLY BY
Inches	Centimeters	2.540
Feet	Meters	0.305
Yards	Meters	0.914
Miles	Kilometers	1.609
Square Inches	Square Centimeters	6.451
Square Feet	Square Meters	0.093
Square Yards	Square Meters	0.836
Square Miles	Square Kilometers	2.590
Acres	Square Hectometers	0.405
Cubic Feet	Cubic Meters	0.028
Cubic Yards	Cubic Meters	0.765
Fluid Ounces	Milliliters	29.573
ıts	Liters	0.473
arts	Liters	0.946
allons	Liters	3.785
Ounces	Grams	28.349
Pounds	Kilograms	0.454
Short Tons	Metric Tons	0.907
Pound-Feet	Newton-Meters	1.356
Pounds per Square Inch	Kilopascals	6.895
Miles per Gallon	Kilometers per Liter	0.425
Miles per Hour	Kilometers per Hour	1.609

TO CHANGE	TO	MULTIPLY BY
Centimeters	Inches	0.394
Meters	Feet	3.280
Meters	Yards	1.094
Kilometers	Miles	0.621
Square Centimeters	Square Inches	0.155
Square Meters	Square Feet	10.764
Square Meters	Square Yards	1.196
Square Kilometers	Square Miles	0.386
Square Hectometers	Acres	2.471
Cubic Meters	Cubic Feet	35.315
Cubic Meters	Cubic Yards	1.308
Milliliters	Fluid Ounces	0.034
Liters	Pints	2.113
Liters	Quarts	1.057
ers	Gallons	0.264
ms	Ounces	0.035
ograms	Pounds	2.205
Metric Tons	Short Tons	1.102
Newton-Meters	Pounds-Feet	0.738
Kilopascals	Pounds per Square Inch	0.145
lometers per Liter	Miles per Gallon	2.354
meters per Hour	Miles per Hour	0.621



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